The Road to 450 mm Semiconductor Wafers

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IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Overview

- Why 450 mm Wafers?
- Technical Challenges
- Economic Challenges
- Solutions
- Summary

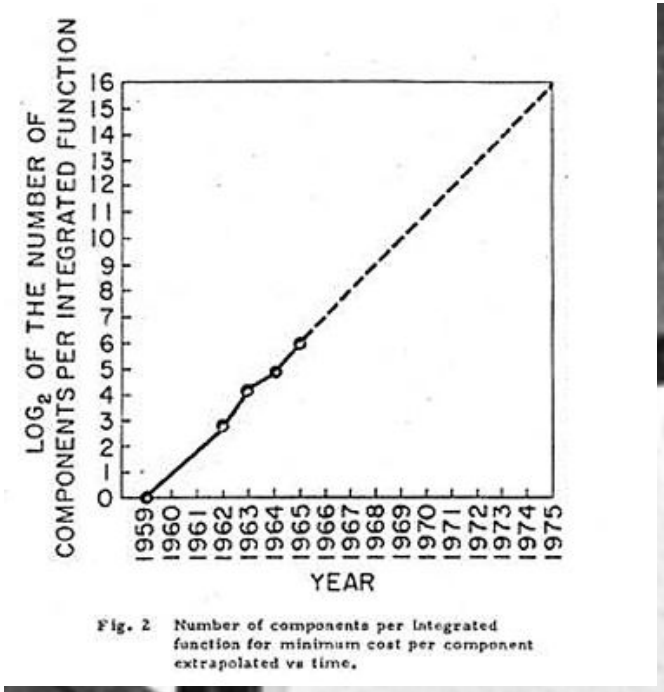


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

… the number of transistors on a chip will double approximately every ~~year~~ two years …

Gordon Moore 1962 credit: Fairchild Camera & Instrument Corporation.

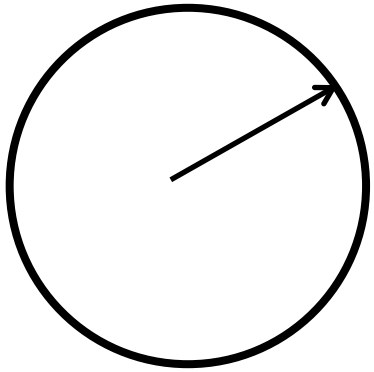
Electronics, Volume 38, Number 8, April 19, 1965
The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph on next page). Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.



$A = \pi r^2$

$r' = 1.5r$

$A' = 2.25A$

If cost' = 1.125 cost

$$\frac{\text{cost'}/A'}{\text{cost}/A} = 0.5$$

Economics again!

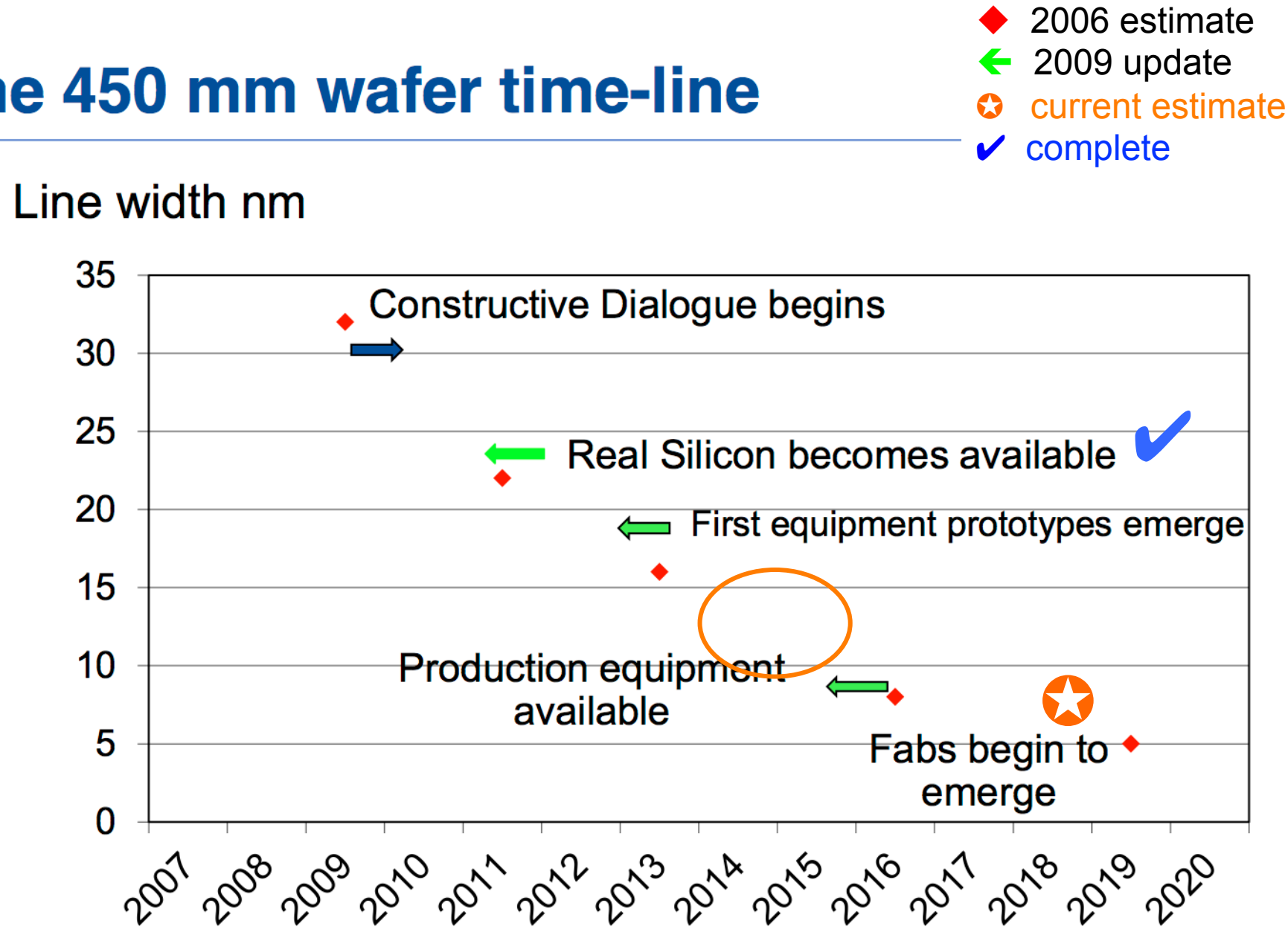
If the total incremental cost of manufacturing a wafer 1.5 times the previous size is held to 12.5%, the cost per area for the larger wafer is half.

≈ 1 process node

Intel 200 → 300 mm

> 30% per die cost reduction

The 450 mm wafer time-line



Dean Freeman, "The Shift to Mobility", SEMI SV Lunch Forum, April 19, 2012

Gartner

TECHNICAL CHALLENGES

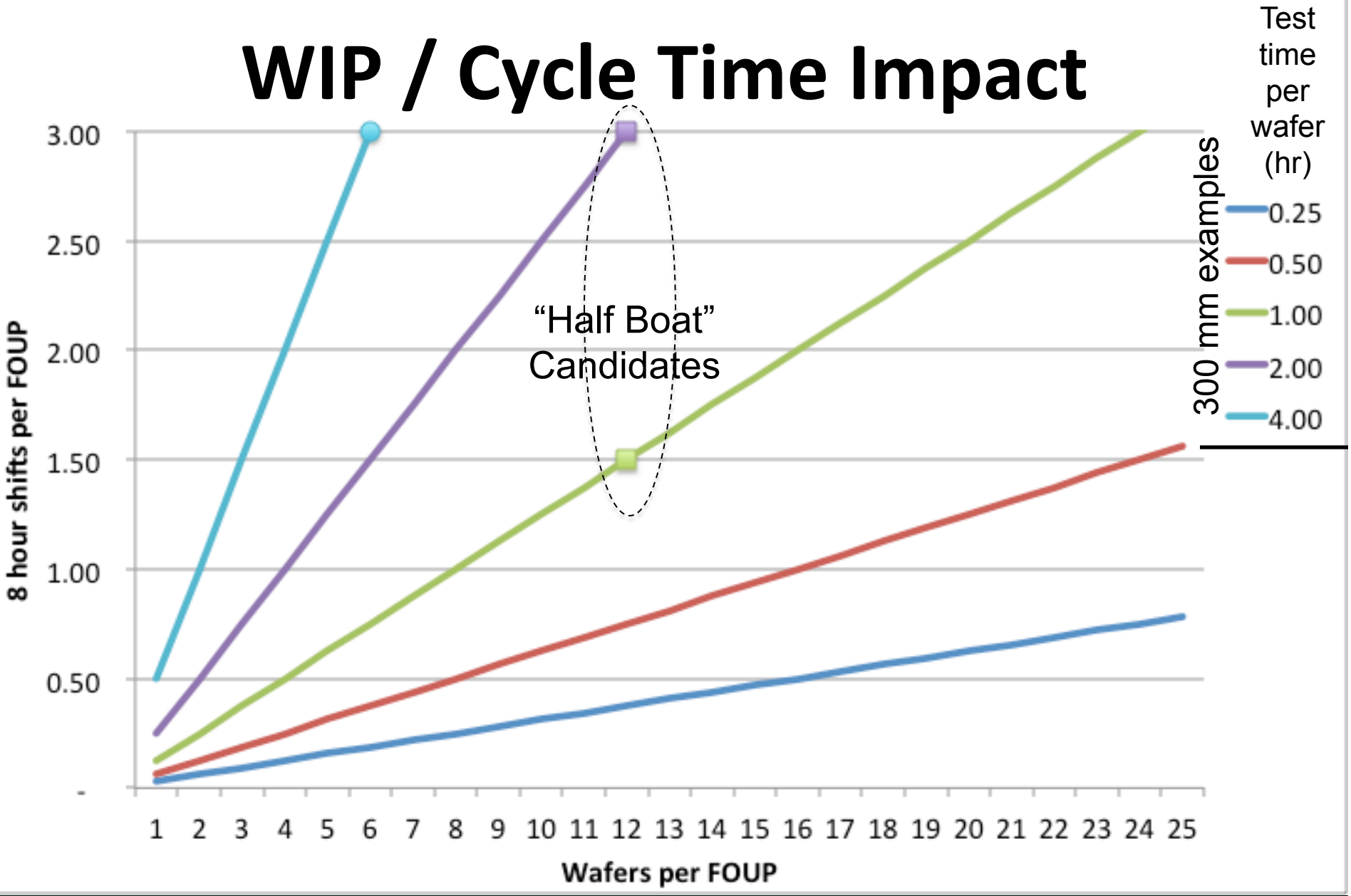
Prober - Direct Scale Up?

1.5x

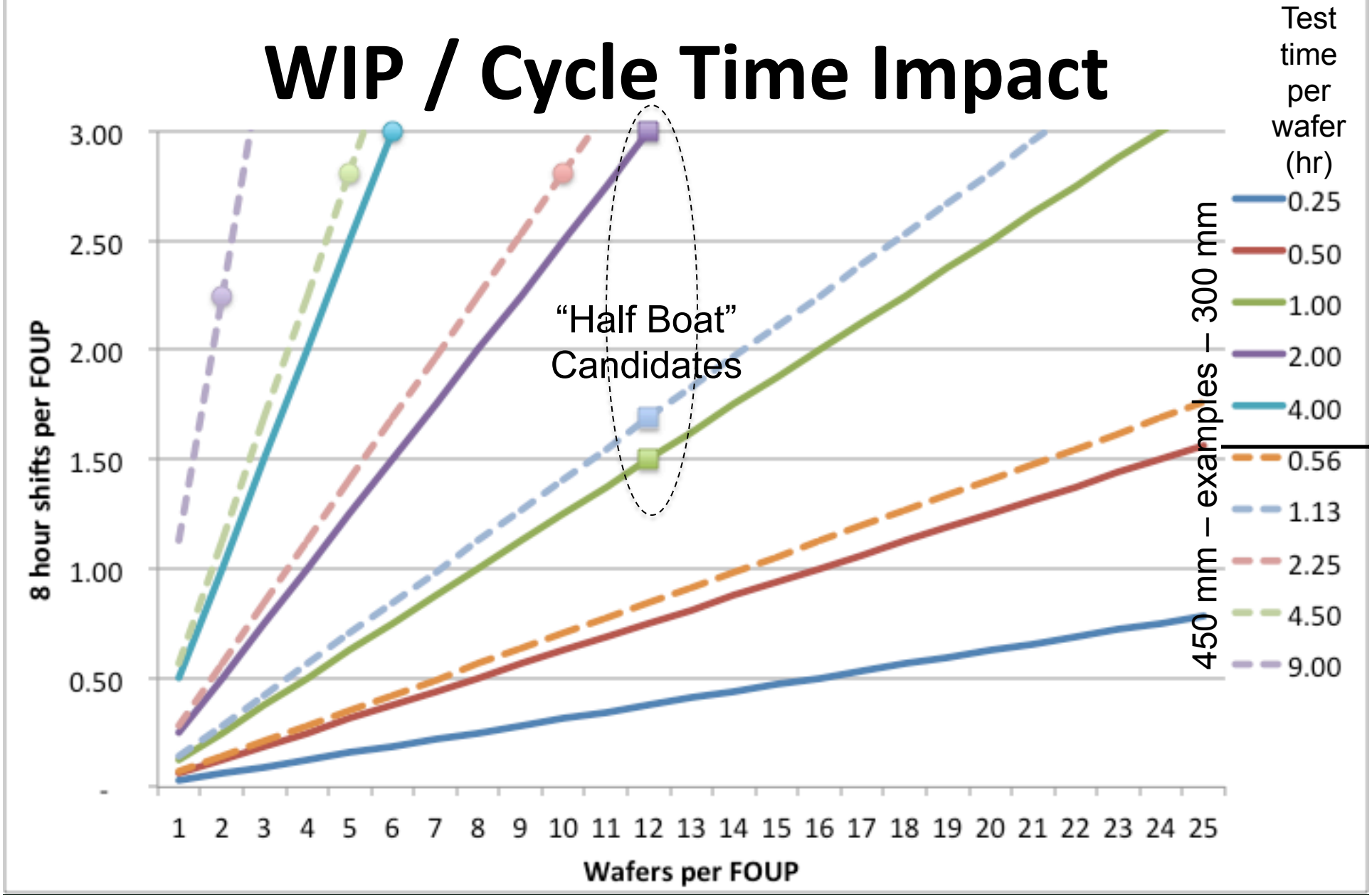
Accretech

Dimensions	1450 w x 1775 d x 1420 h mm	Dimensions	2175 w x 2663 d x 1420 h mm ?
Weight	1500 kg	Weight	3375 kg ?

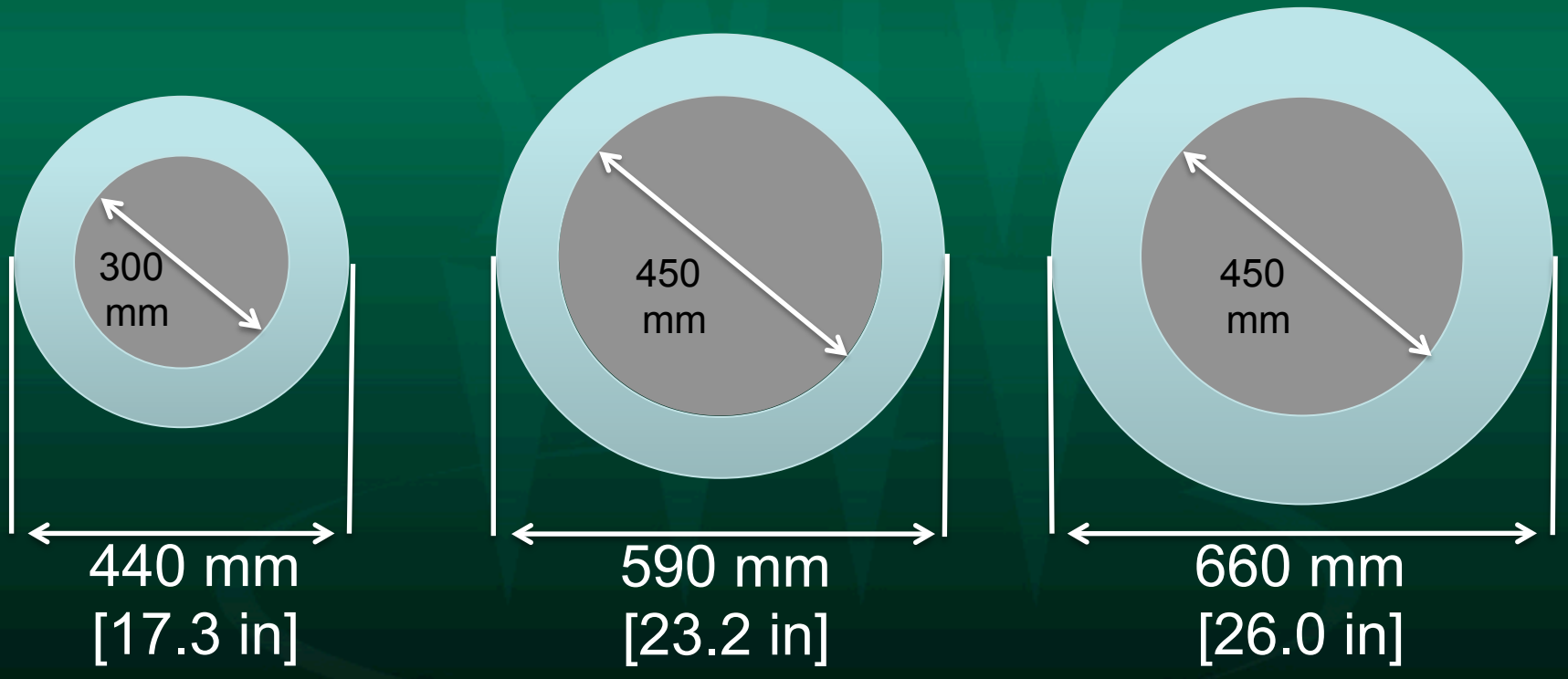
WIP / Cycle Time Impact



WIP / Cycle Time Impact



Very Large Printed Circuit Boards (PCB)

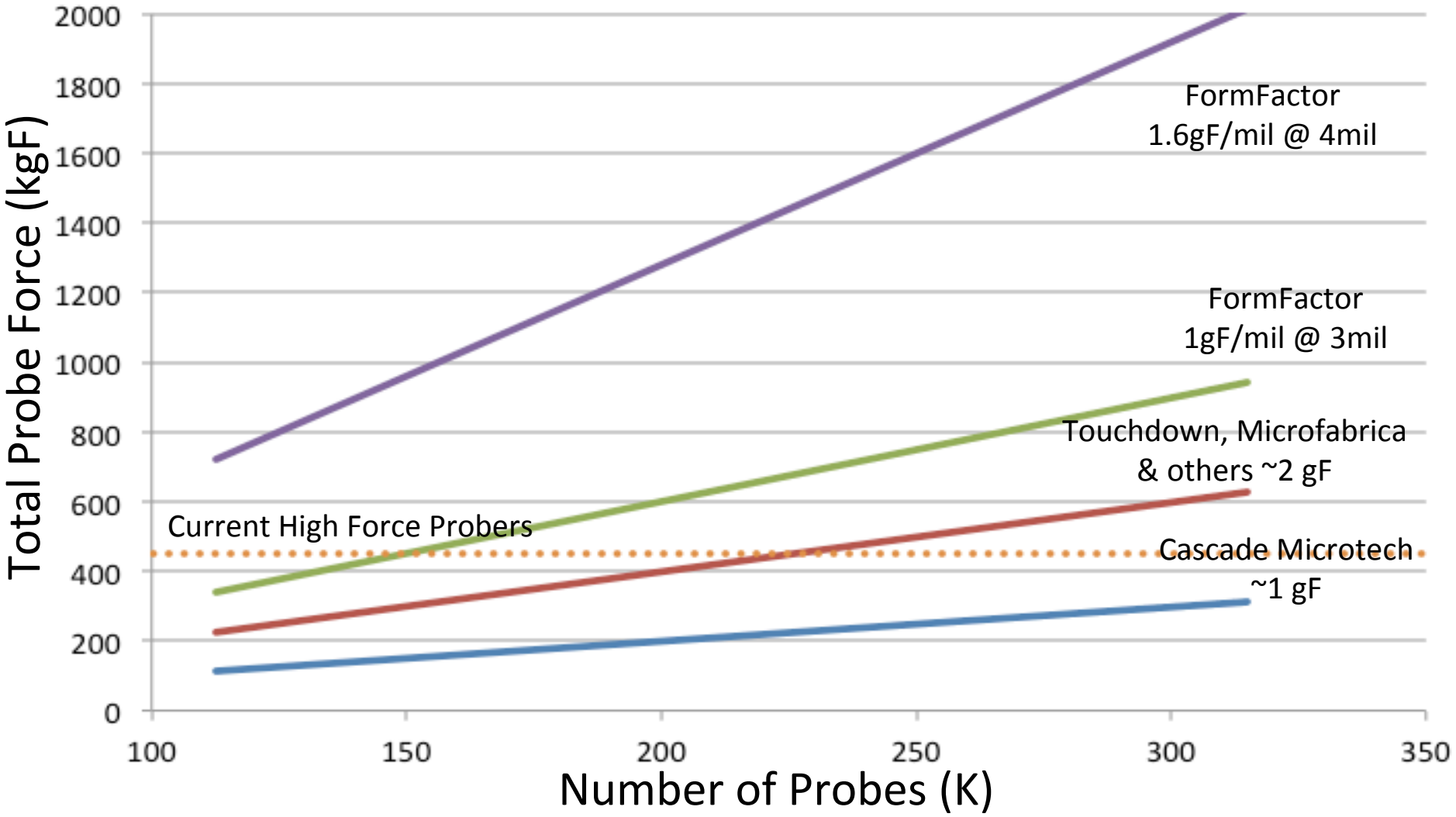


Current DRAM tester

Same connector area width

Connector area increased by 2.25x for additional signals

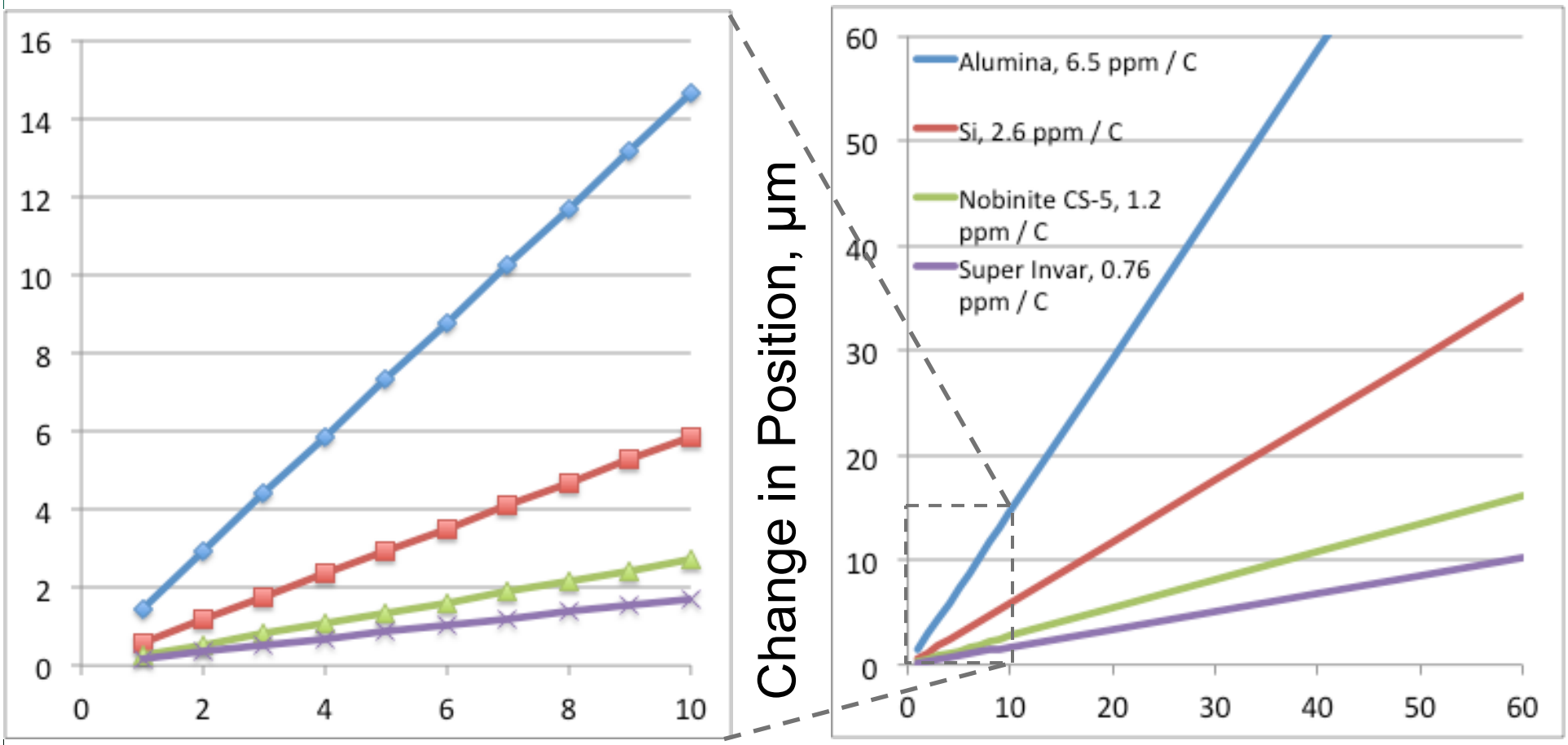
Probe Force



Marinissen – IMEC / Cascade Microtech 2011; Losey – Touchdown Technologies 2010; Huebner – FormFactor 2009; Folk – Microfabrica 2008

Operational probe movement

Probe card operating range



Please see notes on next page

- **Assumptions & notes**
  - Wafer chuck & wafer are at desired temperature
    - Stable due to active thermal management of chuck.
    - Wafer heats up “instantly” due to low relative thermal mass and pre-heating.
  - Calculations are worst case at wafer edge r=225 mm
  - Probe movement is predominantly thermal movement of probe card
    - Probe card heats and cools as heat source (chuck) moves away to perform operations unless active thermal management is implemented.
    - Different stiffener / structural materials are listed.
    - Actual coefficient of thermal expansion (CTE) of probe card typically higher due to high CTE of PCB and other materials.
  - First order calculations of thermal positioning effects in plane (X & Y) only, there are significant other factors including movement of probe card in Z, warping, and thermal stress that need to be considered.
- **Calculations**
  - First order thermal movement of probe at edge of probe card (worst case):
    - Delta Probe Position = r * delta Temperature * CTE
  - Operating range:
    - Delta Temperature = (maximum hot temperature – maximum cold temperature) / 2
    - Example: hot = 100 C, cold = -20 C ➔ delta T = 60 C, card designed scaled for nominal 40 C.
- **Recent papers addressing thermal movement include**
  - Daniels – Texas Instruments SWTW 2011
  - Lee – GigaLane SWTW 2011
  - Breinlinger – FormFactor SWTW 2009
  - Boehm – Feinmetall SWTW 2009
  - Harker – FormFactor SWTW 2009

ECONOMIC CHALLENGES

OPEX + CAPEX → ¢/die

Only

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Serial Fab Processes:

- Photolithography reticle stepping
- Ion Implantation
- Metrology & inspection
- Non-full wafer test

Larger Probe Cards =

- Higher Material & Processing Costs
- New NREs
- New Equipment

Yield – larger area requires lower defect density or cost effective rework.

Feldman SWTW 2011

Non Recurring Engineering Expense

Architecture	Design	Tester	Customer
R&D	NRE	NRE	NRE
Design Input	X		X
Probes			?
Guide Plates	X		
Space Transformer	X		
Interposer	?		
PCB Design	X (External?)	X	?
PCB Fab	External	?	?
Mechanical H/W	?	X	?
Electronics	?	?	?
Metrology	X	X	?
Packaging		X	?

Advanced Process Technology

Cost Drivers

Process Steps
Masks
Substrates
  Material
  Active Area
Yield
  Defect Density
  Layers
Equipment
Rework / Repair

Intel

made it simple last time:

Relative Capital Cost <= 1.3
Relative Footprint <= 1.0

$$\text{Relative } X \equiv \frac{X(300)}{X(200)} * \frac{OutputCapacity(200)}{OutputCapacity(300)}$$

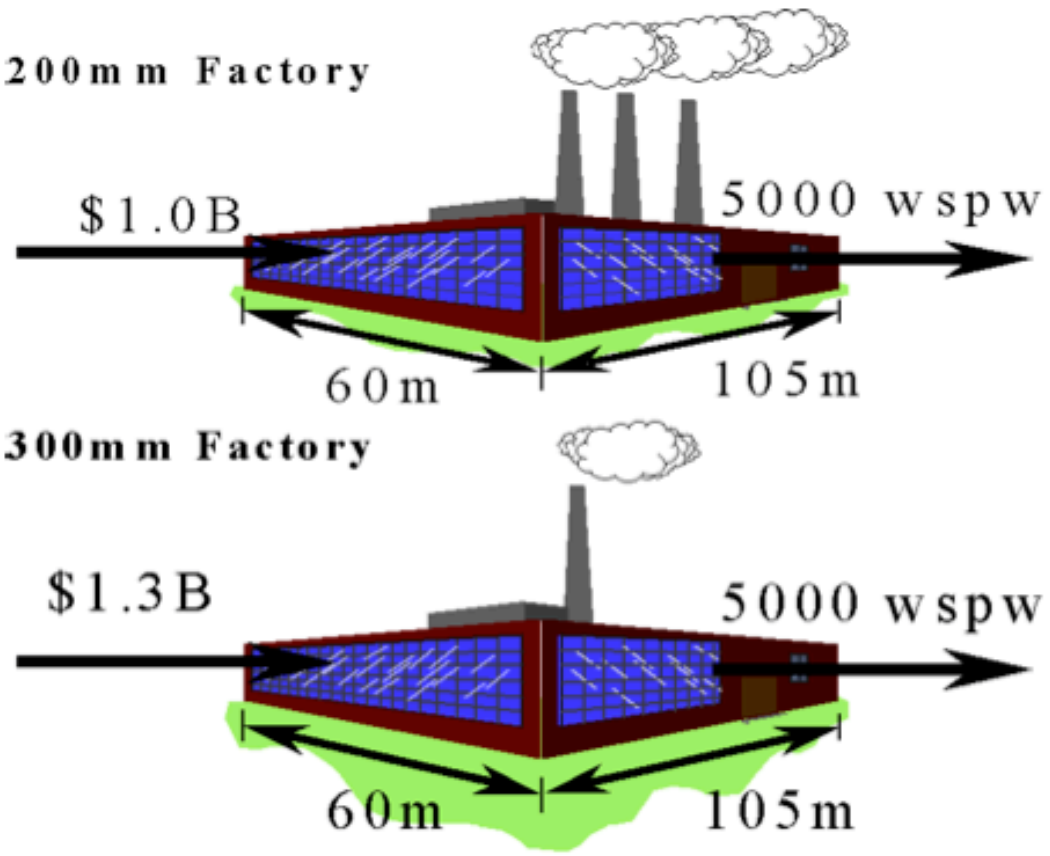


Figure 2: The macro view of the 300mm vision in which 200mm and 300mm factories are compared

Seligson

Mike Splinter, SEMI ISS, January 17, 2012

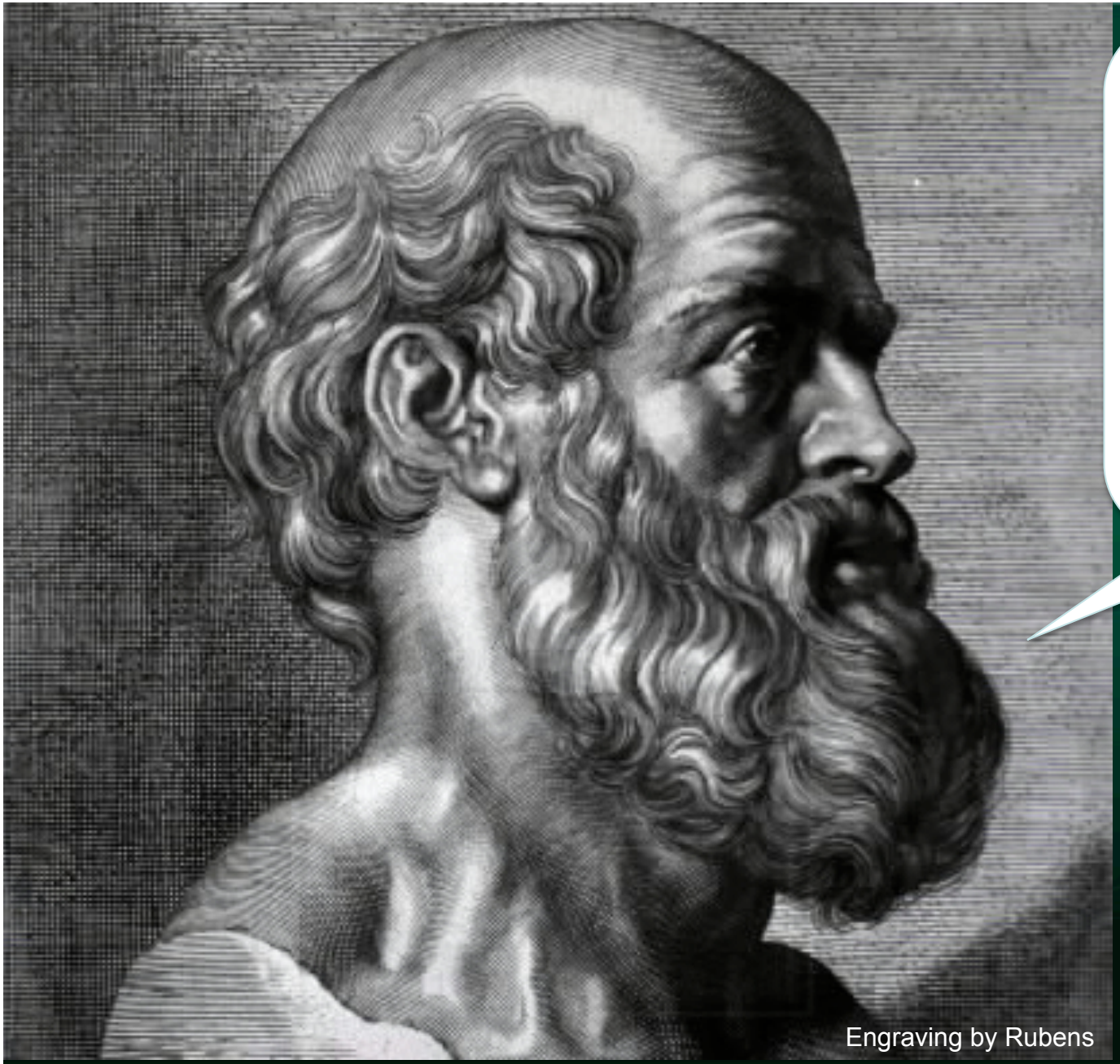
	TOTAL INVESTMENT	TIME TO RECOVER INVESTMENT
300mm development cost for equipment industry[1]	$12B	14 yrs
450mm development cost for equipment industry[2]	$15B - 20B	?? yrs

Synchronized **Roadmap** and **ROI Cadence** are critical

1 Source: VLSI Research 2006
2 Source: Applied Materials estimate

APPLIED MATERIALS®

SOLUTIONS



Engraving by Rubens

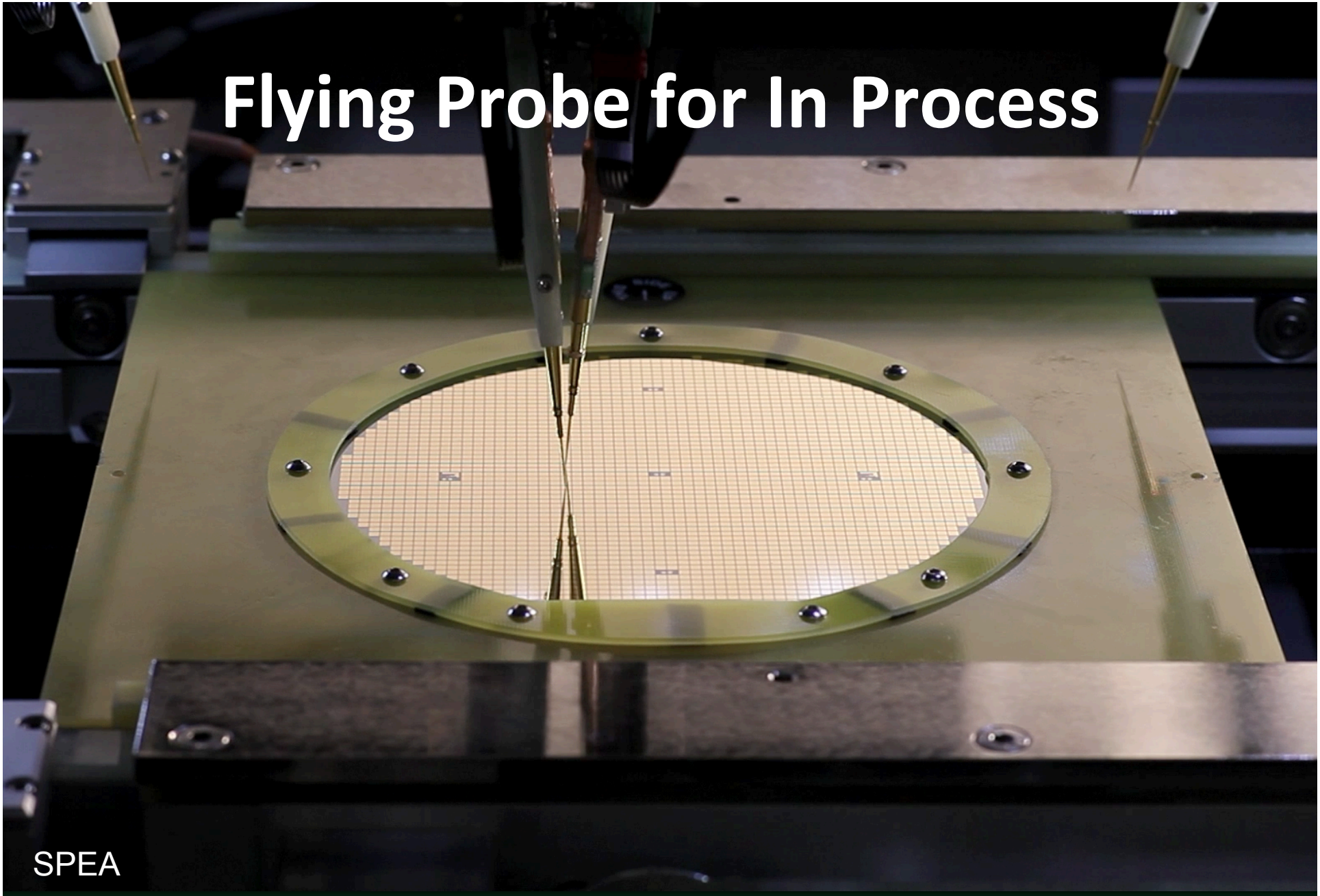
For extreme diseases, extreme methods of cure, as to restriction, are most suitable.

Hippocrates
ca. 460 – 370 BCE

Possible Solutions

Location	Type	Research & Development	Short Term (delayed investment)	Long Term
In Fab	In Process / Parametric	Semi-automatic probe station	Flying probe	Super-sized wafer prober
Post Fab	Single to medium multisite	Quartered wafers	Reconstituted wafers	Super-sized wafer prober Test in Tray
	Full wafer contact (1-10? TDs)			Simplified prober / restricted movement

Flying Probe for In Process



SPEA

Possible Solutions

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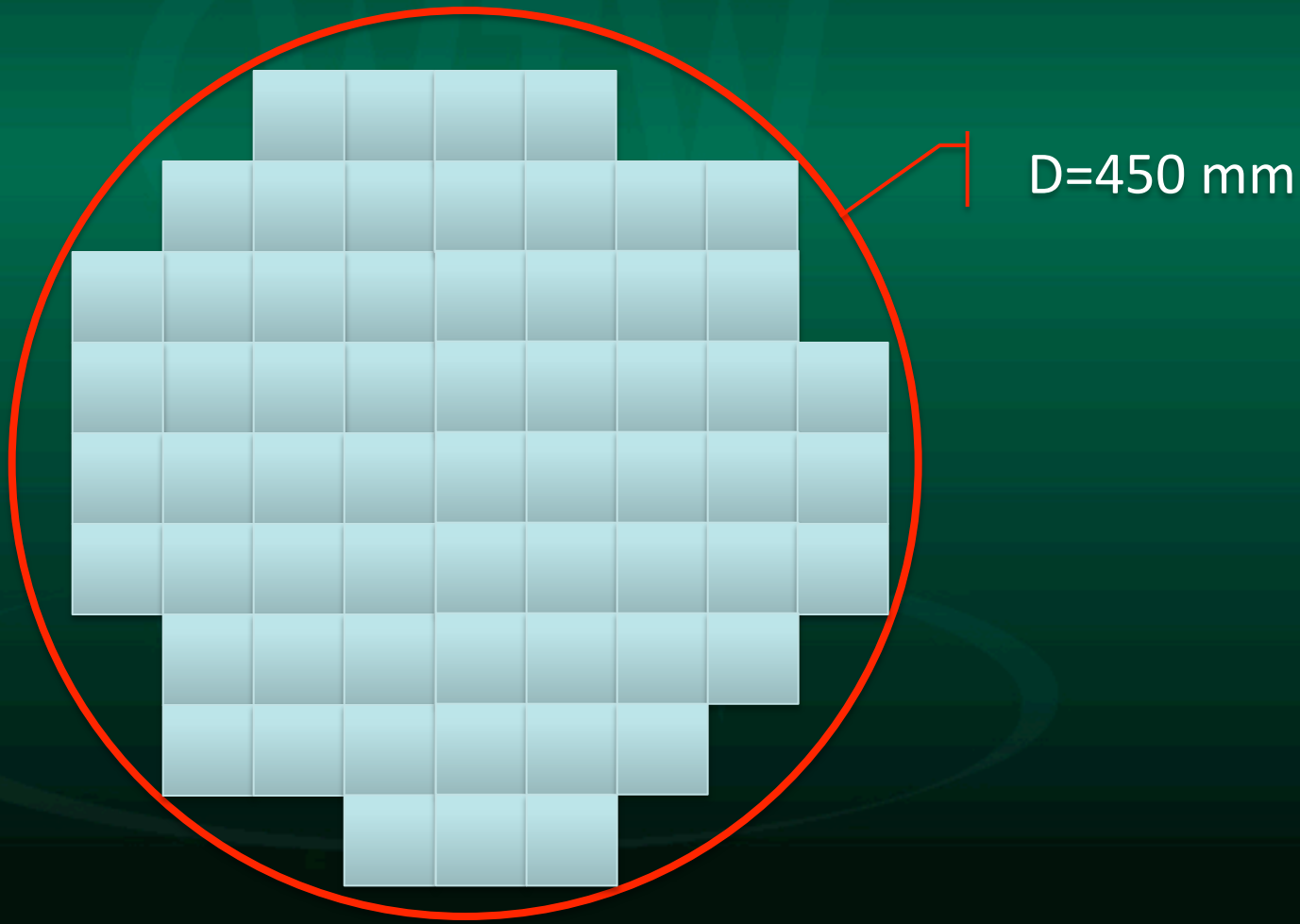
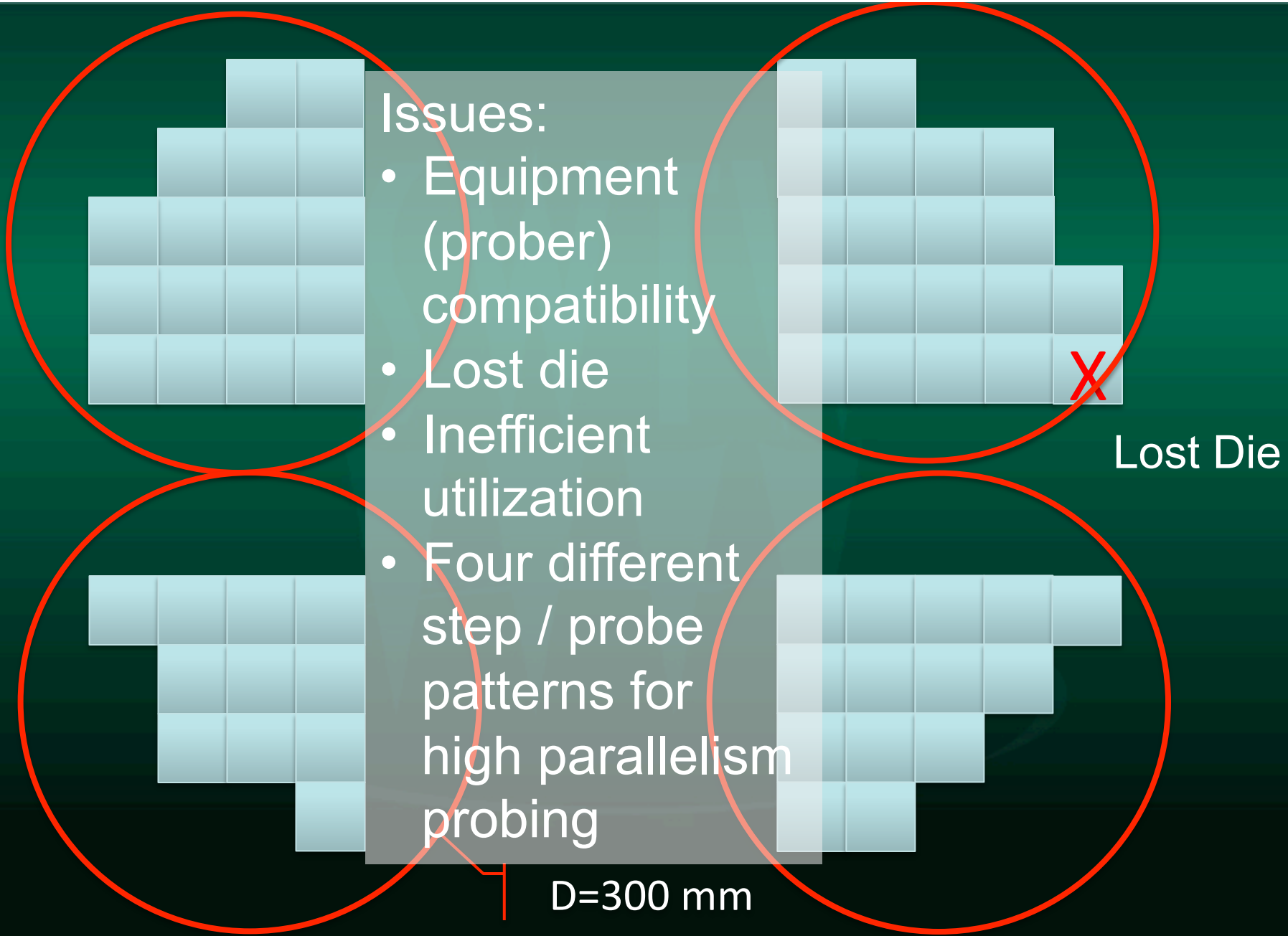
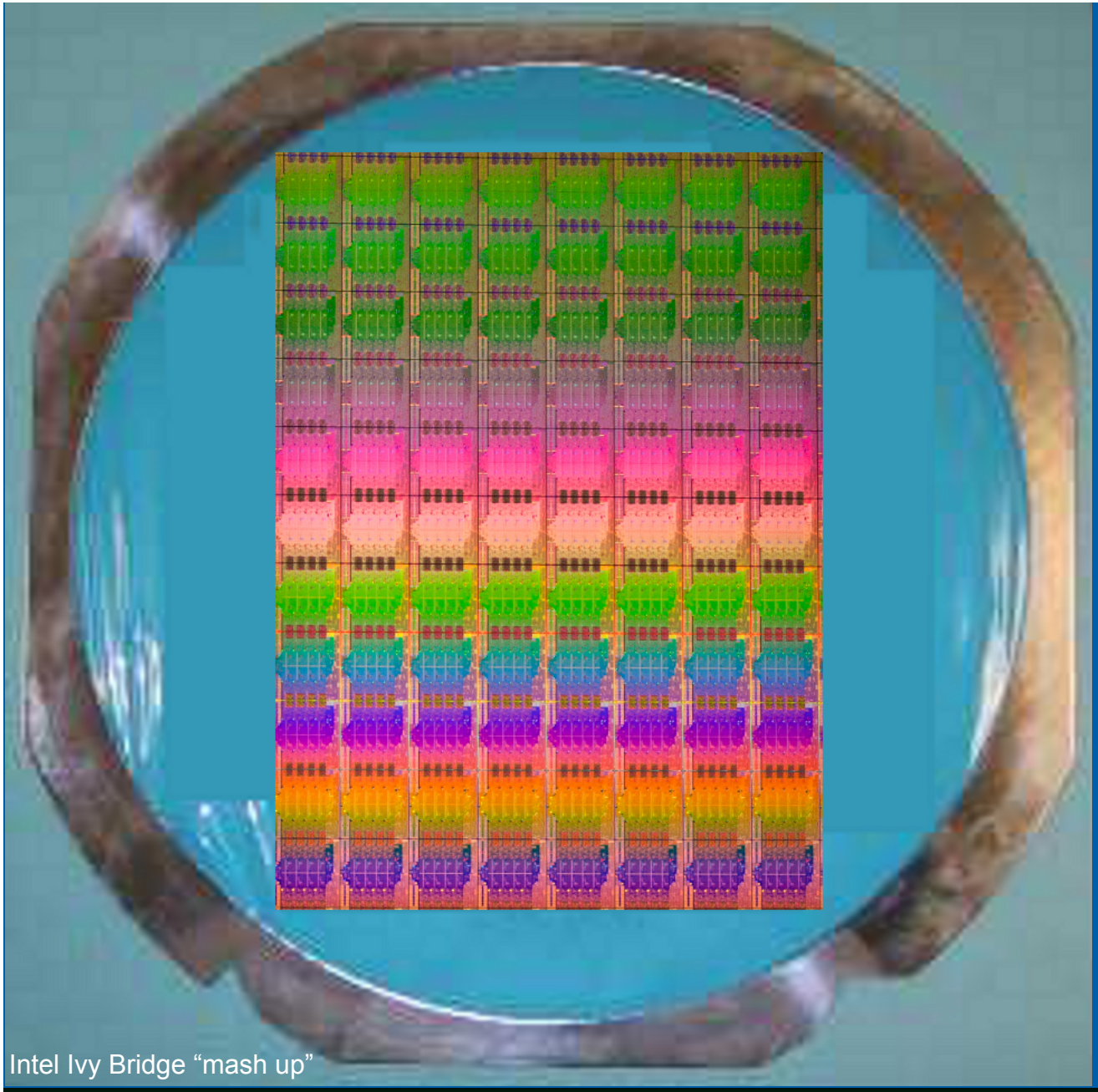
Quarter the Wafer?




Issues:
• Equipment (prober) compatibility
• Lost die
• Inefficient utilization
• Four different step / probe patterns for high parallelism probing
X
Lost Die
D=300 mm



Intel Ivy Bridge “mash up”

Reconstituted partial “wafer”

Dice arrayed in efficient probing shape on 300 mm film frame

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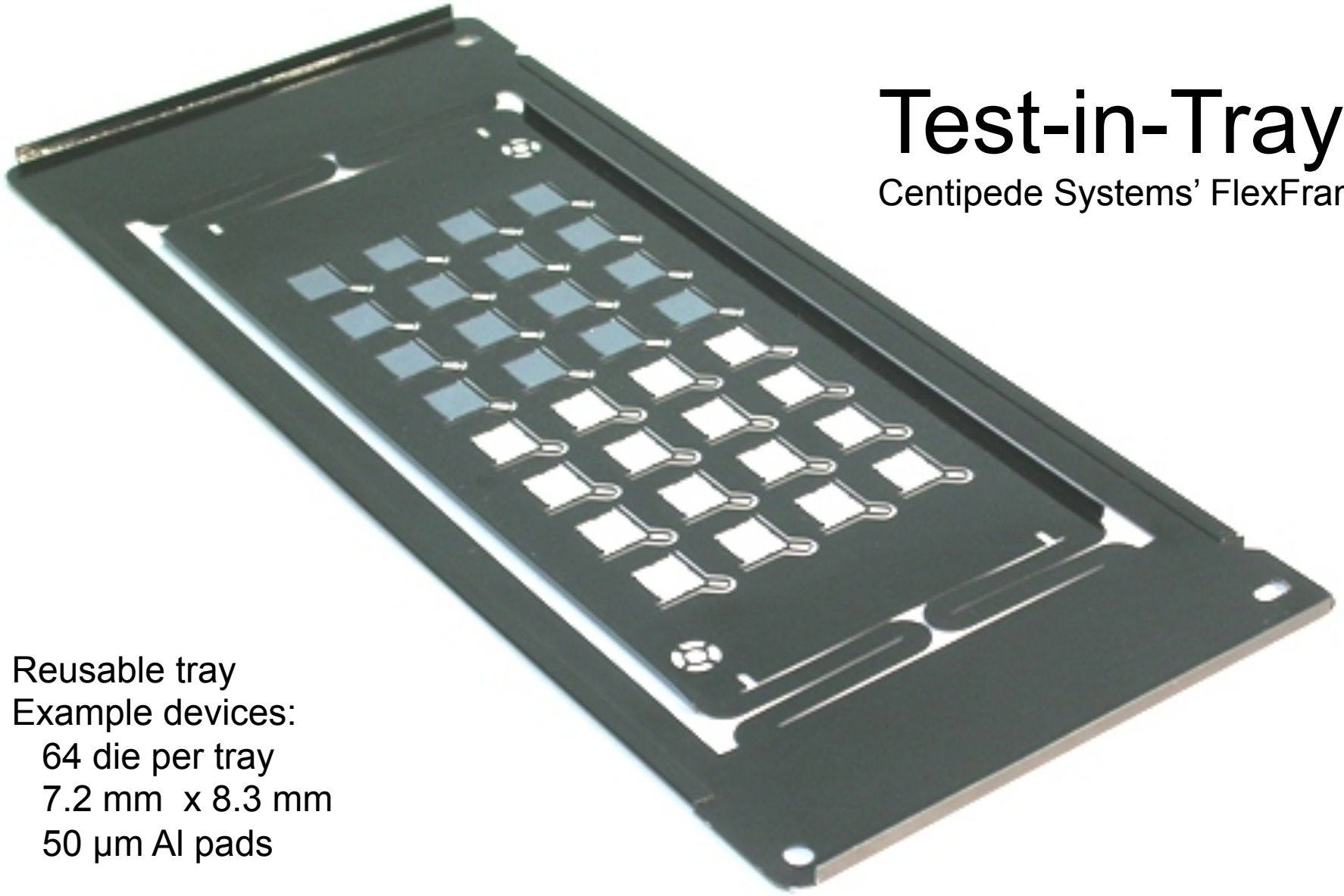
Test-in-Tray

Centipede Systems' FlexFrame



Reusable tray
Example devices:
- 64 die per tray
- 7.2 mm x 8.3 mm
- 50 µm Al pads

Centipede Systems

See also: Test in Tray: Thomas Di Stefano - BiTS 2012

Possible Solutions

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In Fab	In Process / Parametric	Semi-automatic probe station	Flying probe	Super-sized wafer prober
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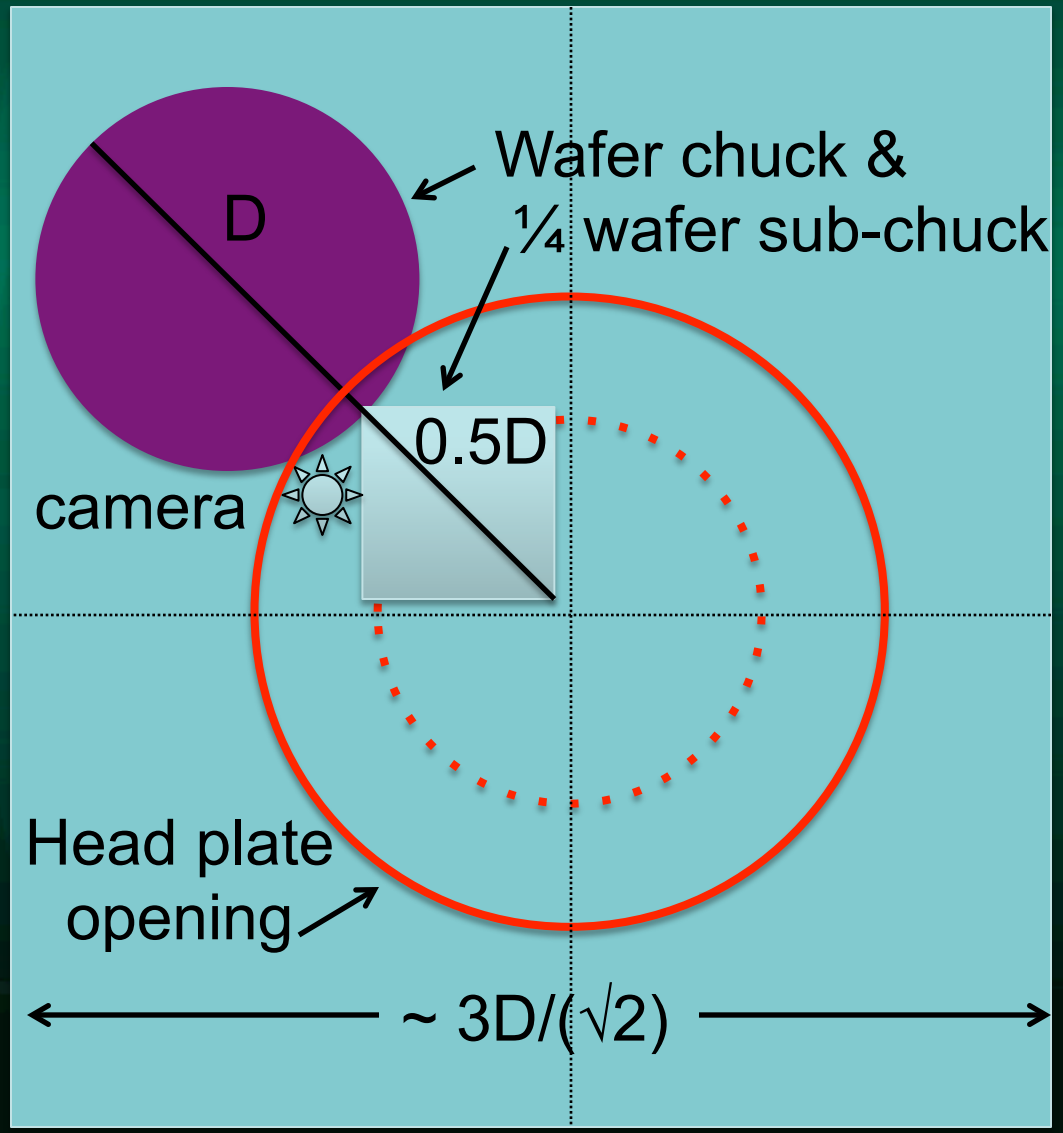
Chuck Area

Minimum chuck area is approximately:

D = 300 mm → 636 mm sq.
D = 450 mm → 955 mm sq.

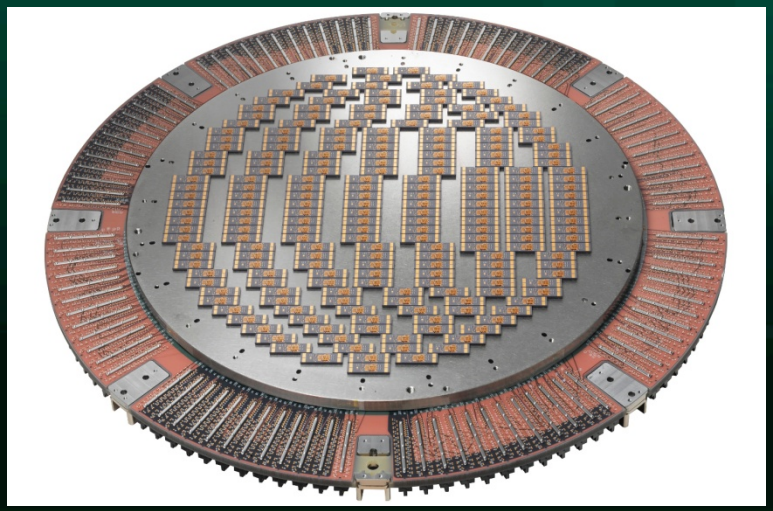
to reach center of head plate opening with all die, sub-chuck, & camera.



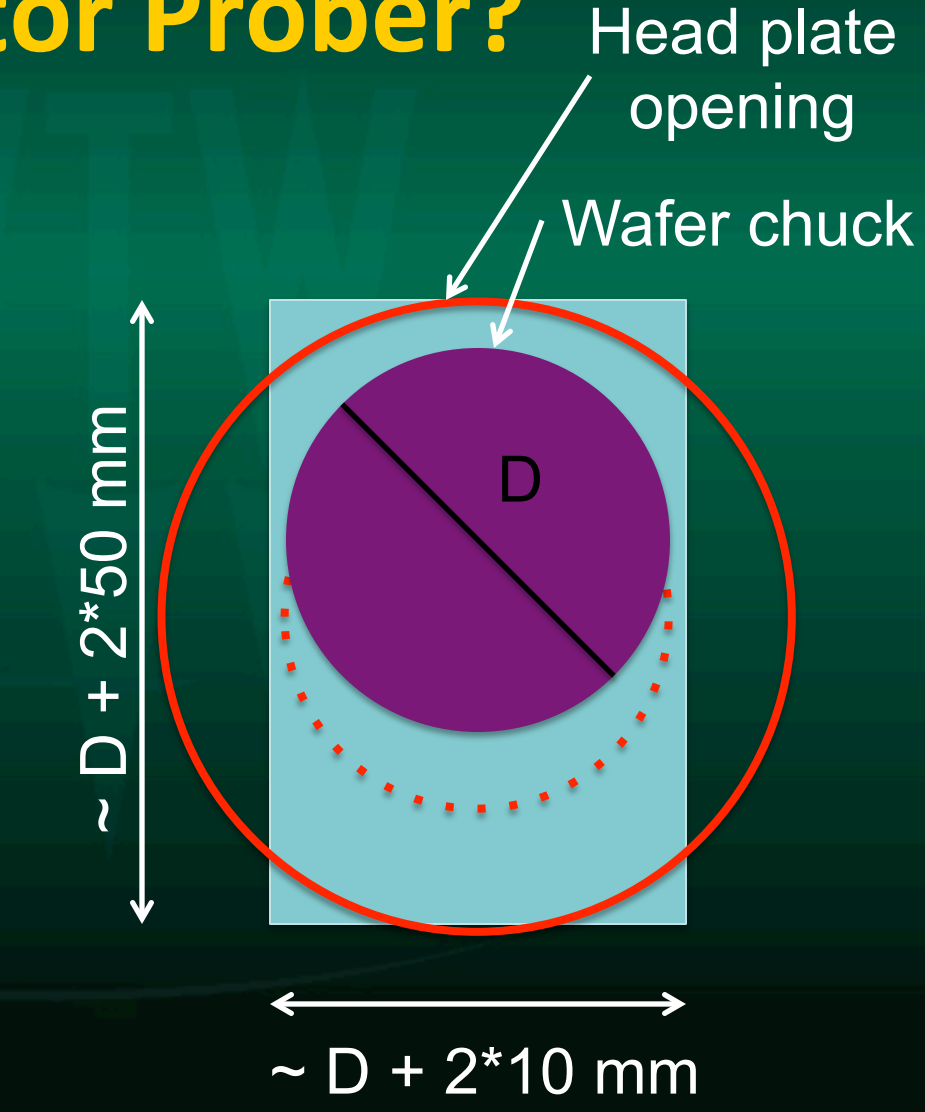
Full Wafer Contactor Prober?

Prober designed for use with full wafer contactors (FWC) such as 1 TD or "rainbow" probe cards.

Restricted movement to +/- 50 mm Y, +/- 10 mm X?

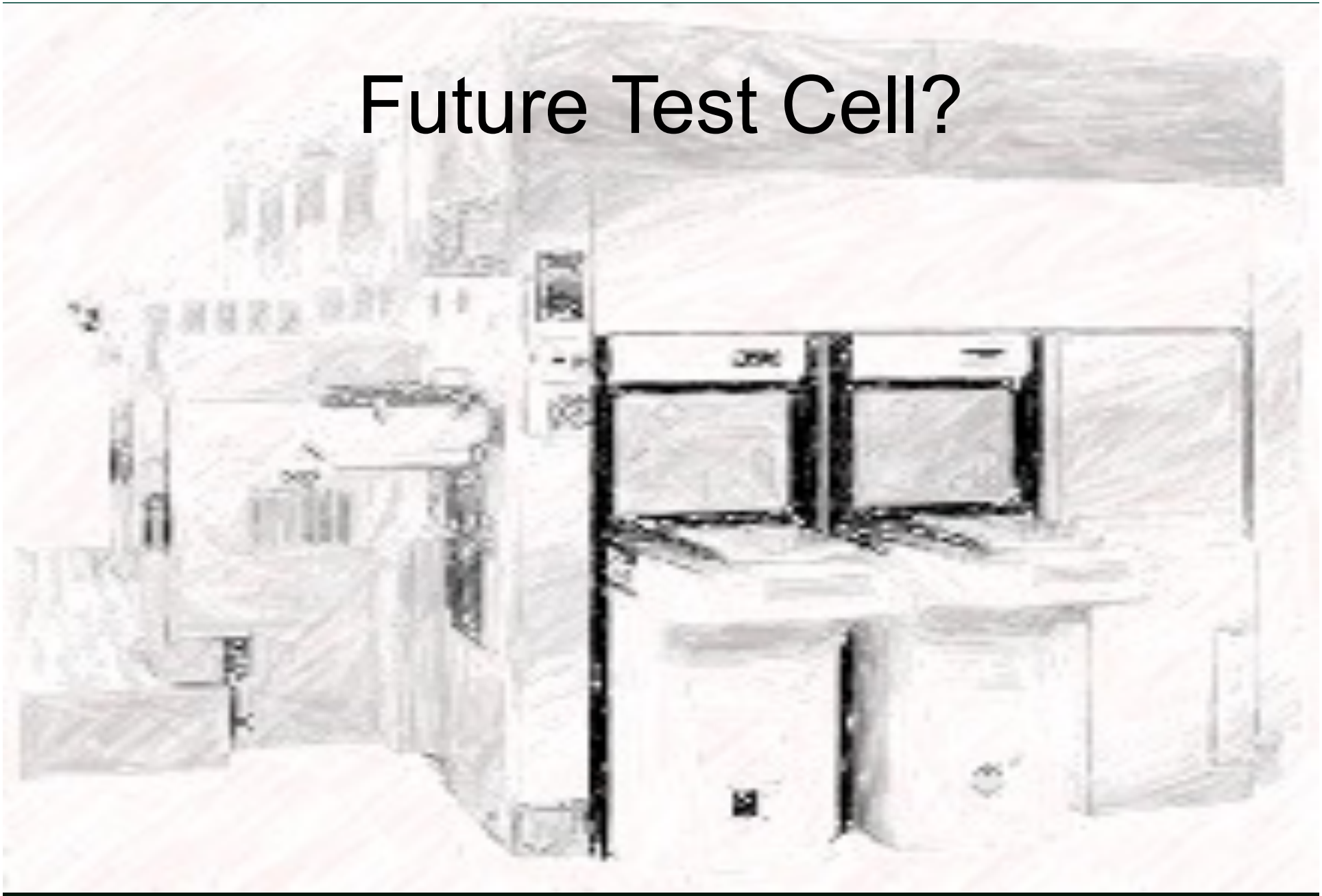


FormFactor SmartMatrix



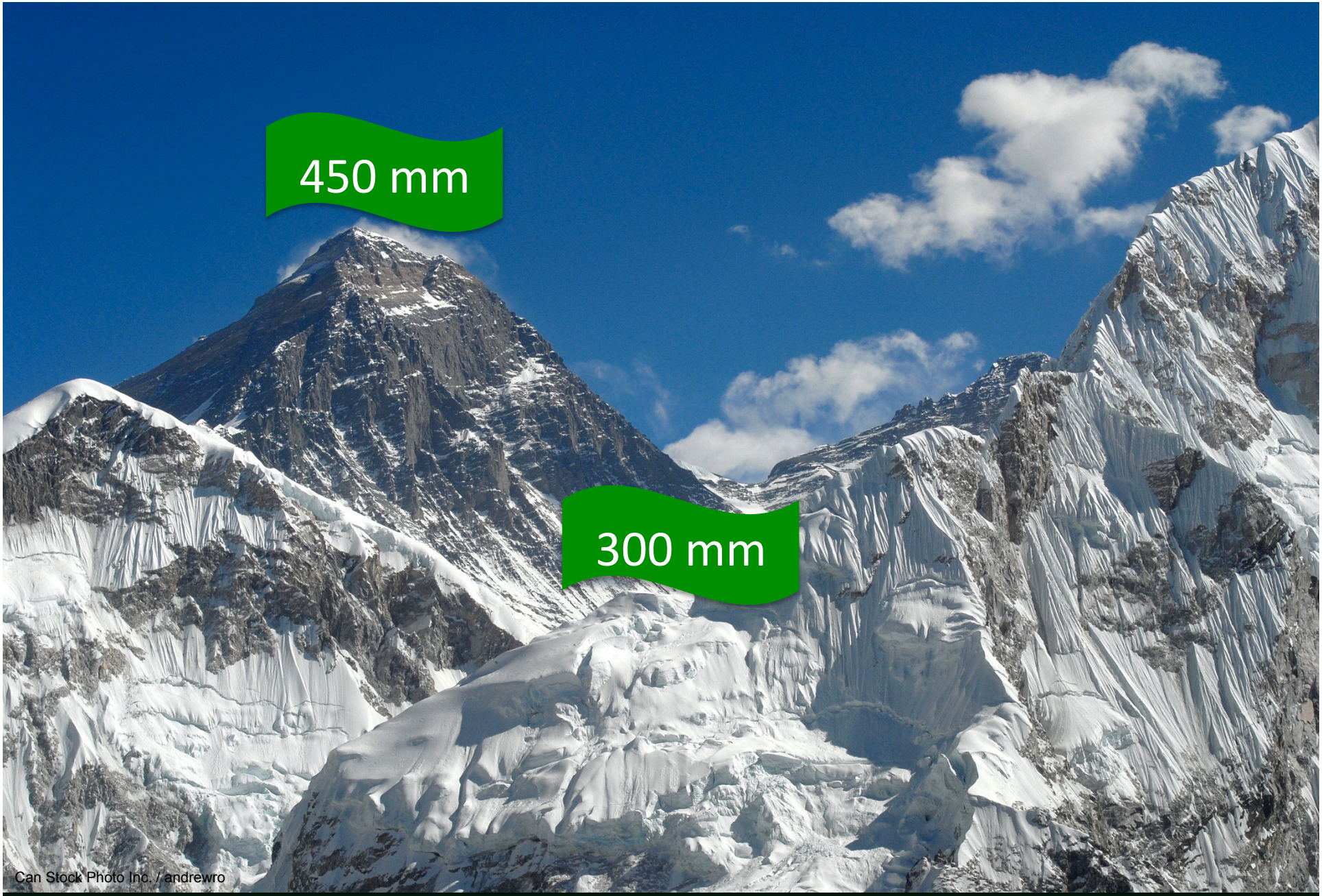
Micronics Japan Co.

Future Test Cell?



Summary

- **Some challenges are 1.5x others are 2.25x**
- **Multiple solutions to technical challenges for R&D, short term, and long term**
  - Need to plan accordingly
- **Largest challenge is financial**
  - Need right solution for each problem with proper return on investment (ROI)
  - Don't want to over invest or "miss the boat"
- **Inflection point enables innovation**


450 mm
300 mm
Can Stock Photo Inc. / andrewro

Acknowledgments

- Accretech
- Applied Materials
- Cascade Microtech
- Centipede Systems
- FormFactor
- Micronics Japan Co. (MJC)
- Multitest
- SPEA
- Tokyo Electron

Thank You!

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Visit my blog

www.hightechbizdev.com

for my summary of SWTW

References

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