Feldman Engineering

2.5D? 3D? What?

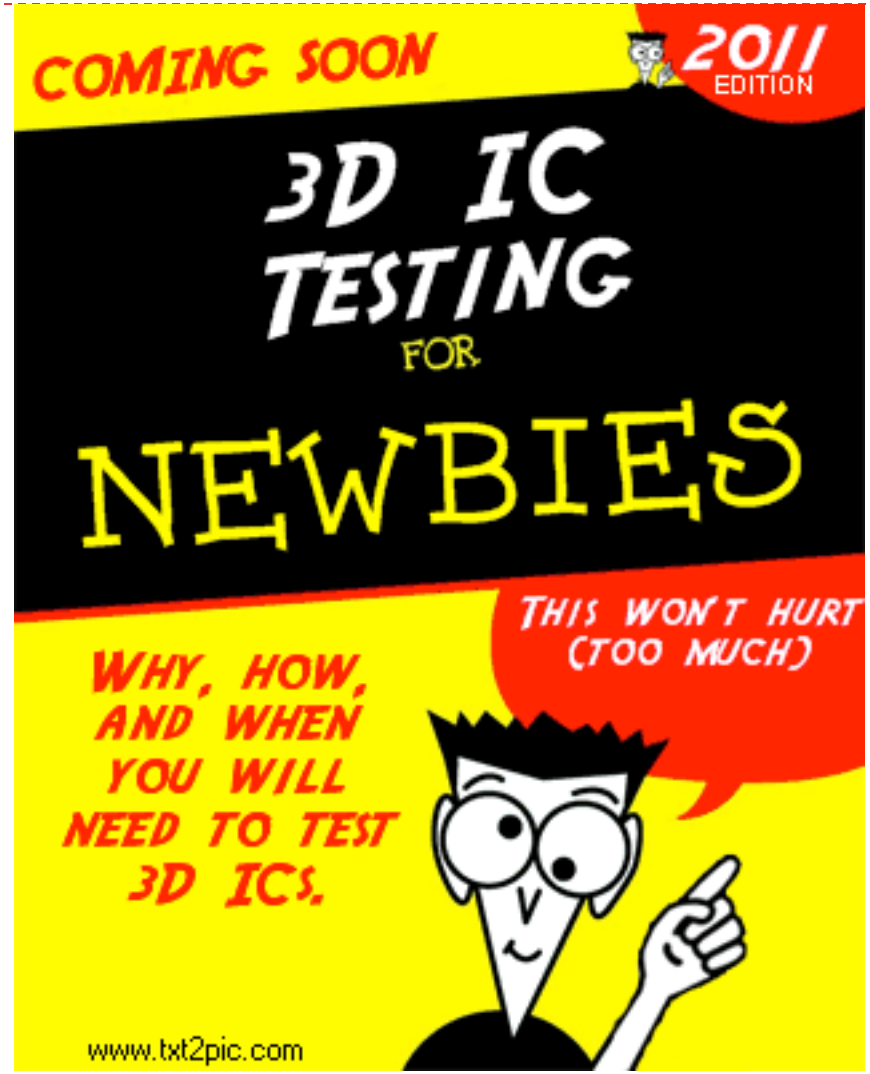
Overview of 3D Integrated Circuit Packaging and Test Challenges

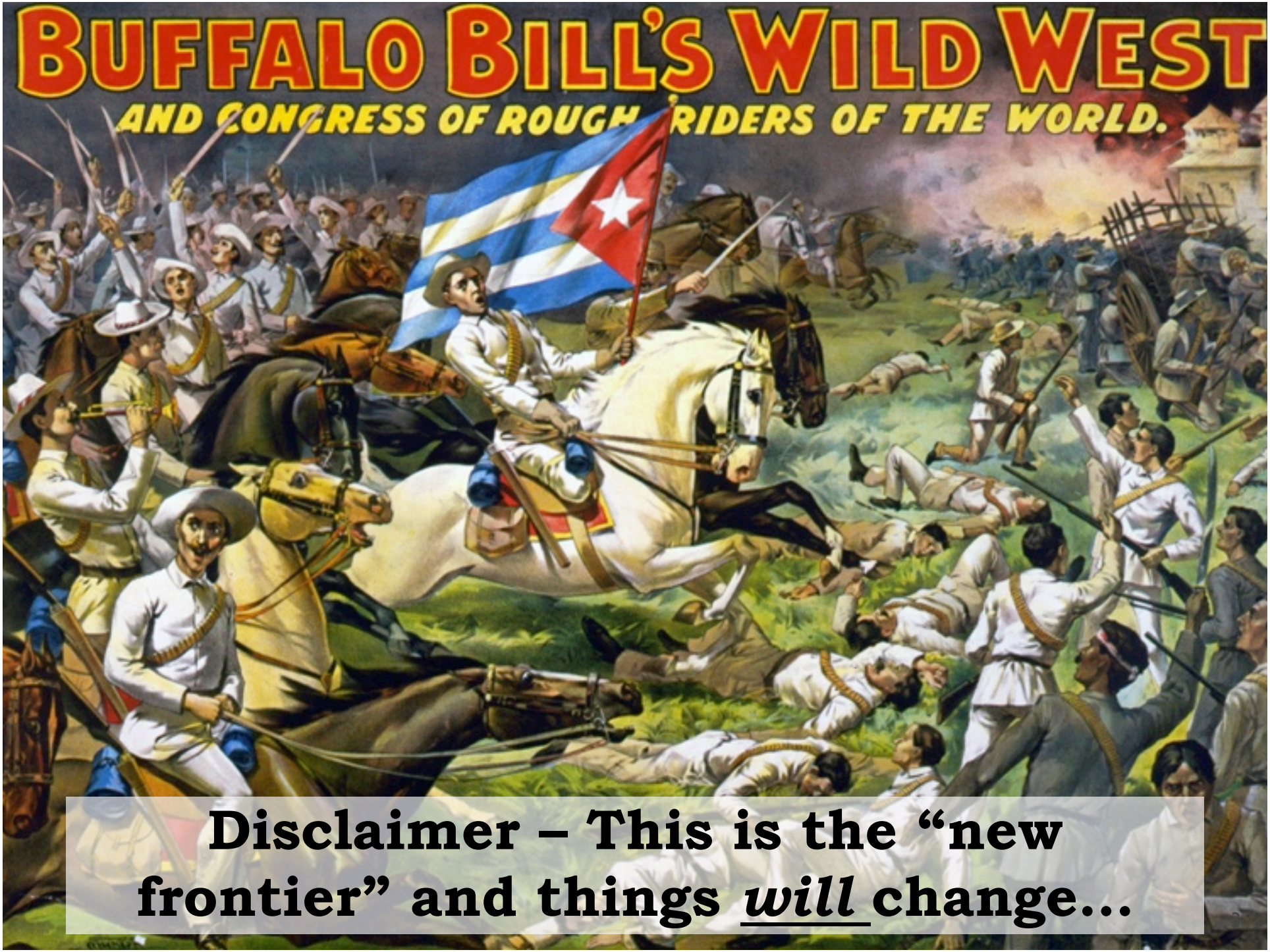
Ira Feldman

November 11, 2010

Outline

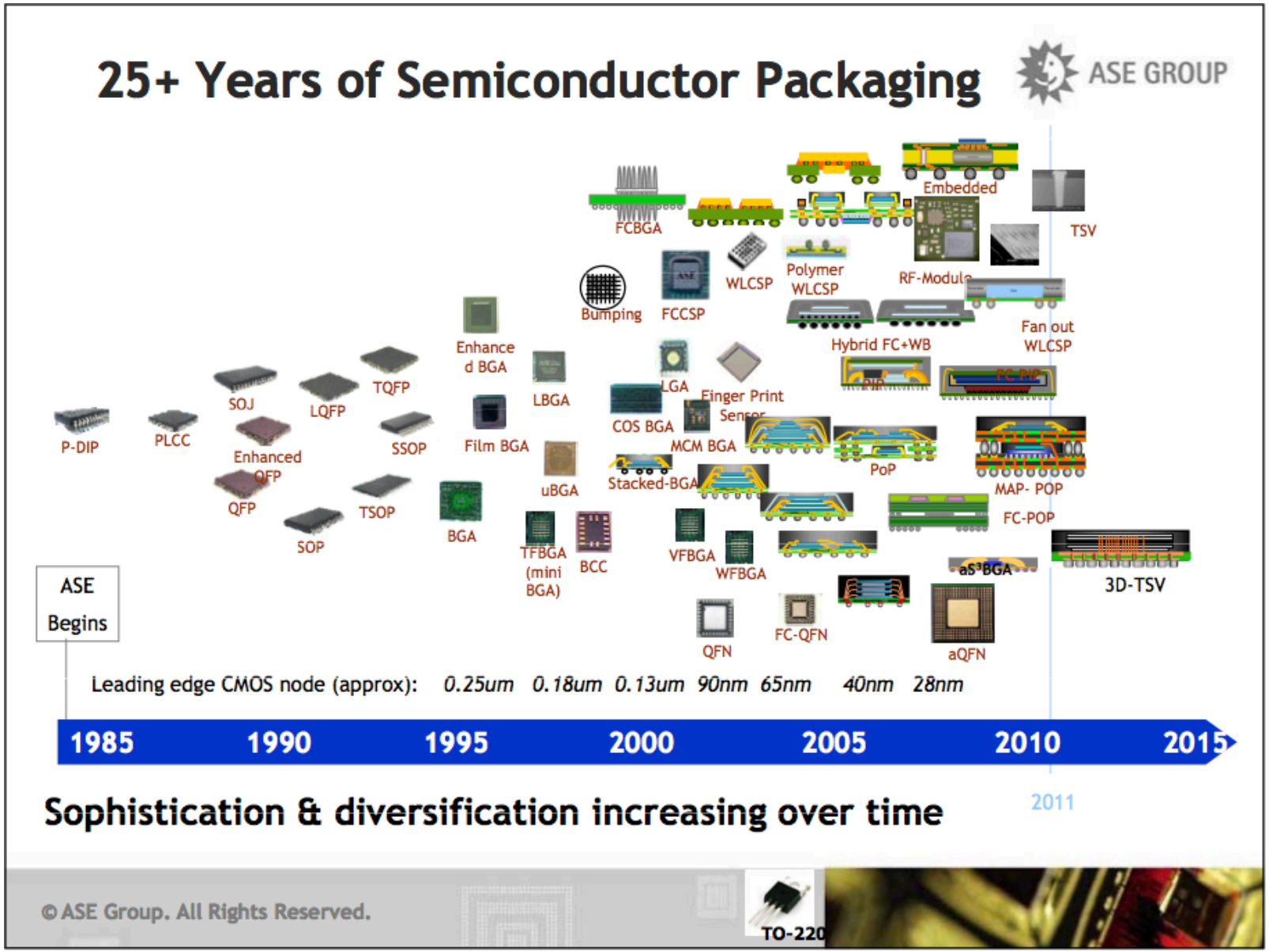
- Why 2.5D & 3D ICs?
- Building stacks
  - TSV Processes
  - 2.5D & 3D stacks
  - Process & Test Flows
- Wafer Probe Solutions
- Key Organizations & Activities
- Future?





Disclaimer – This is the "new frontier" and things *will* change…

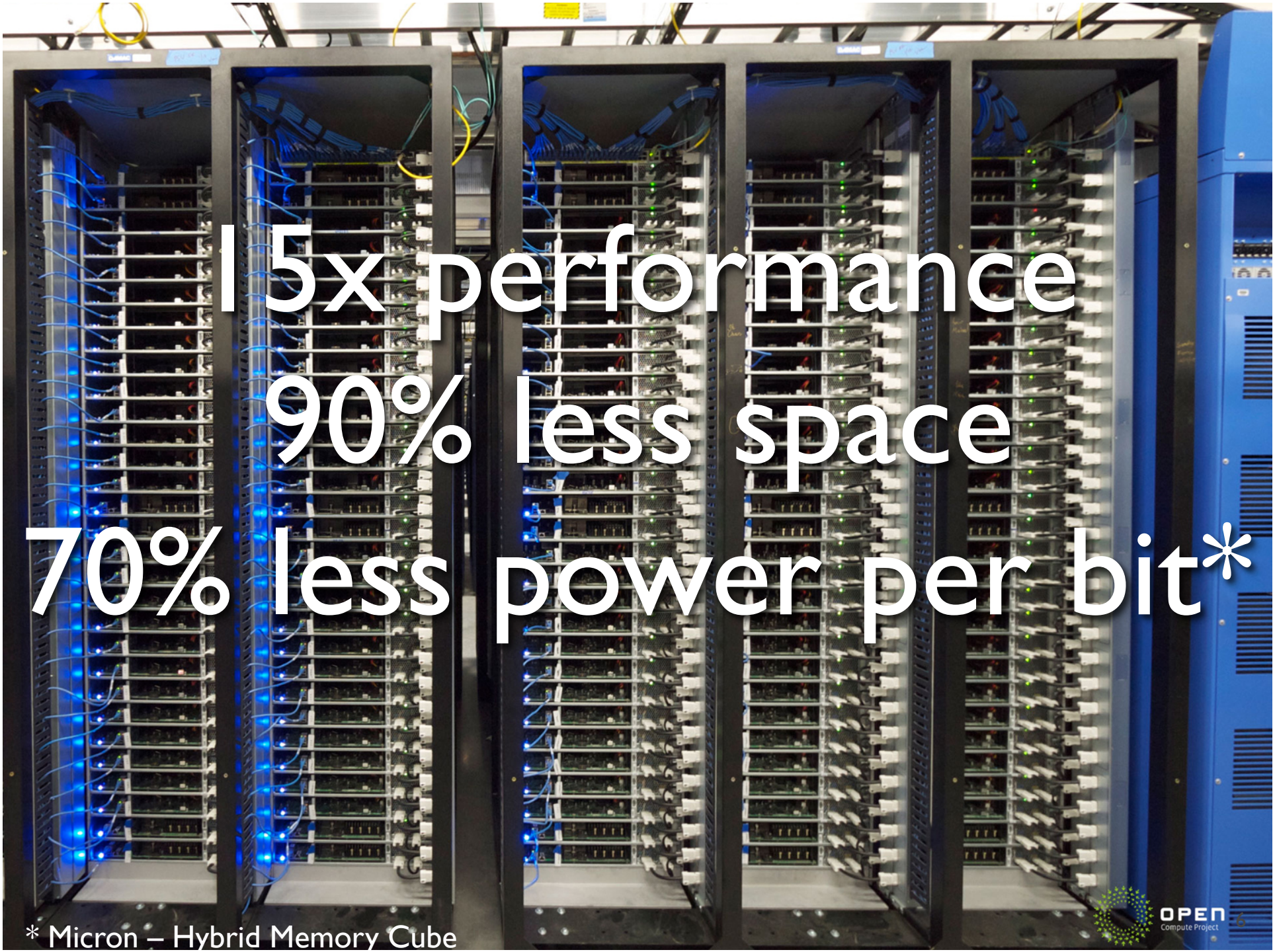
Package Proliferation



"Backend to the Front Line" William Chen, ASE Group, SWTW 2011

Very low power & high density (small volume)

Flickr - blakespot


15x performance
90% less space
70% less power per bit*
* Micron – Hybrid Memory Cube
OPEN
Compute Project

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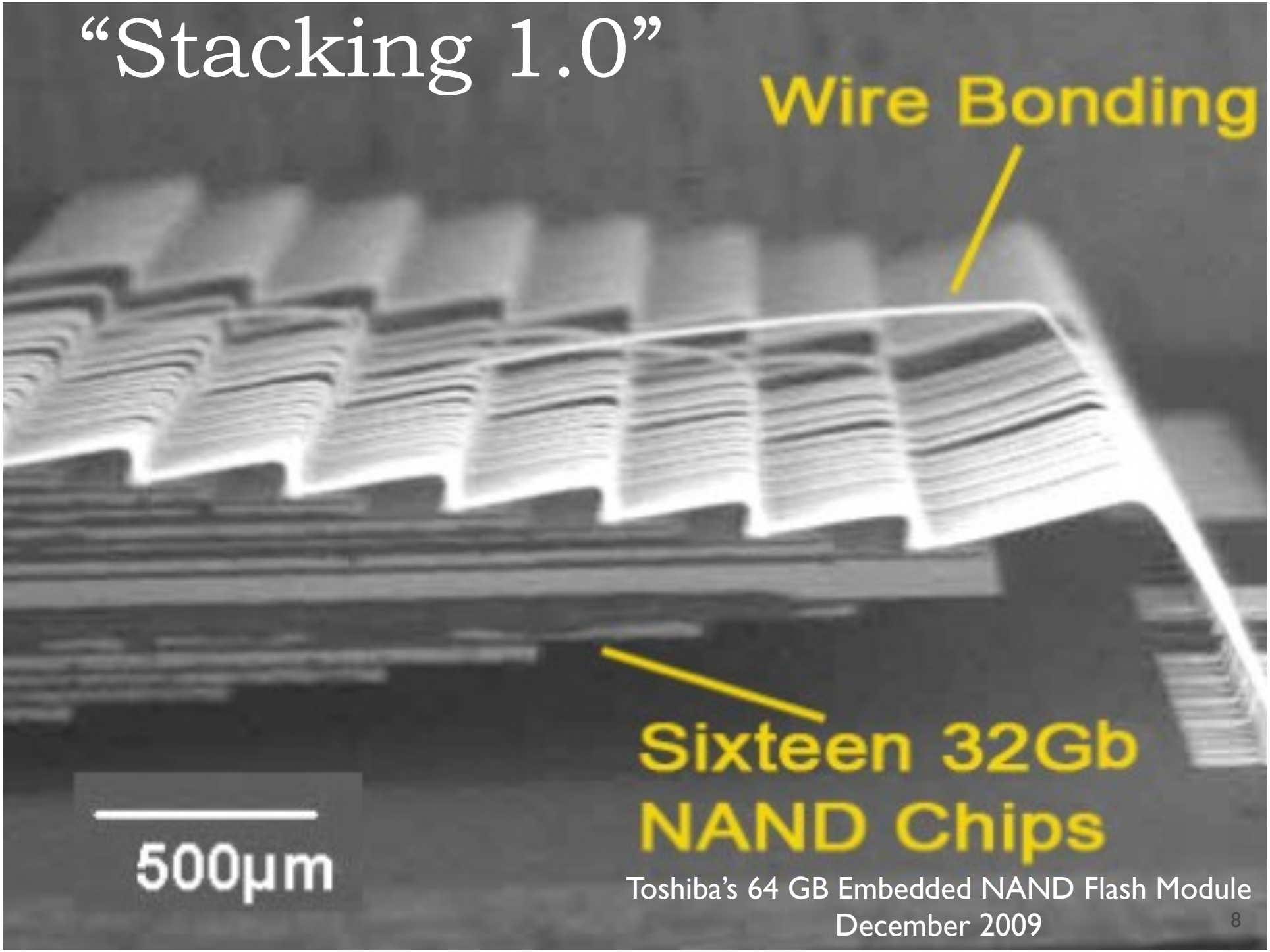
“Stacking 1.0”



Toshiba’s 64 GB Embedded NAND Flash Module
December 2009

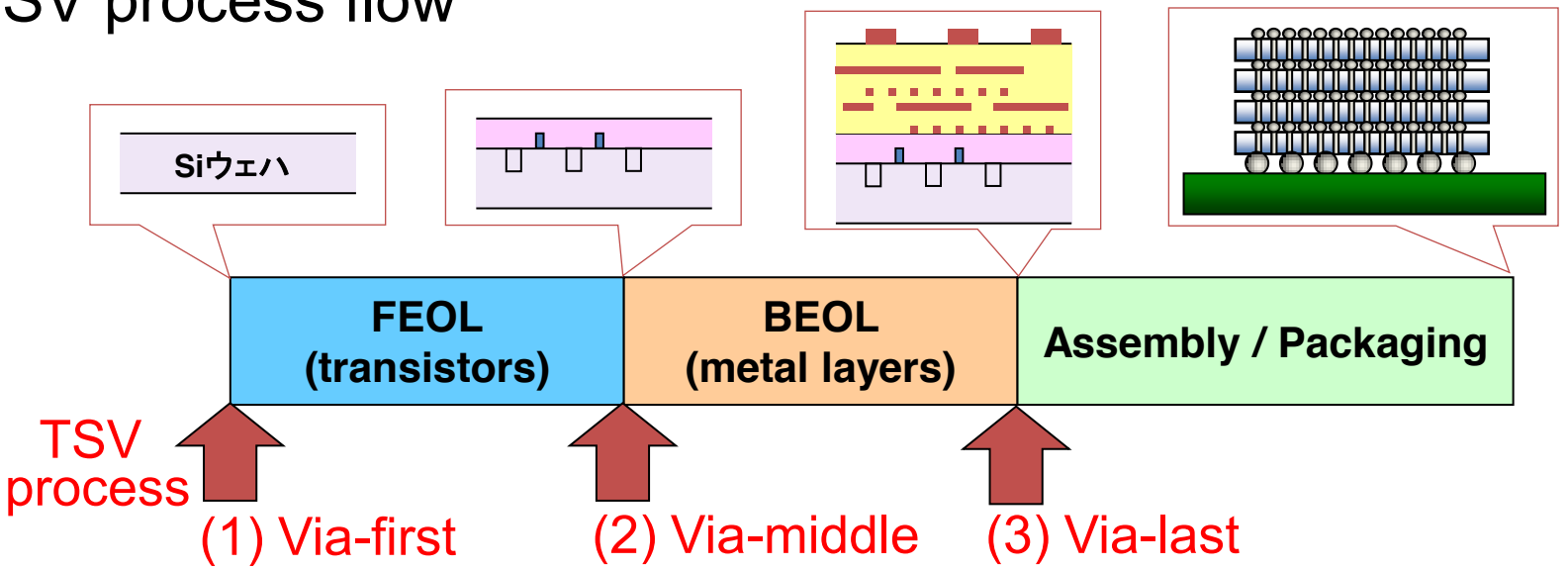
TSV Processing

3D TSV via integration MAIN scenarios

Courtesy of Yole Developpement

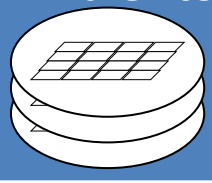
3D integration process options using TSV

◆ TSV process flow



◆ TSV interconnect methods

KGD: known good die

	(1) C2C: chip-to-chip 	(2) C2W: chip-to-wafer 	(3) W2W: wafer-to-wafer 
Pros	Flexible Use of KGD	Flexible Use of KGD	High throughput
Cons	Handling, Bonding	Handling, Bonding	Same chip size, Yield

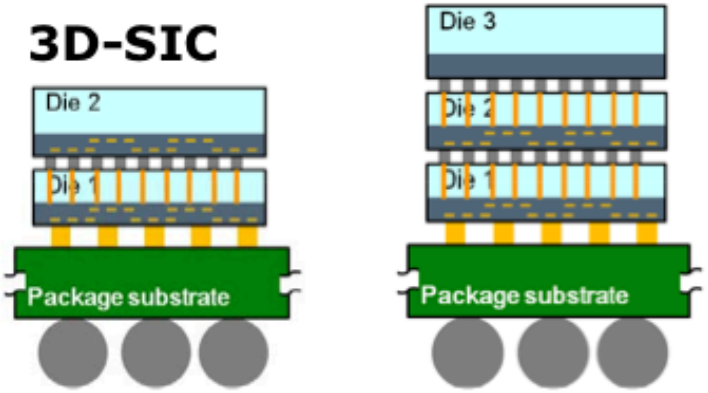
"Panel Discussion: Advanced Packaging and 3D Technologies", Kenichi Osada, Hitachi, 16th Asia and South Pacific Design Automation Conference (ASP-DAC) 2011

Die Stacking

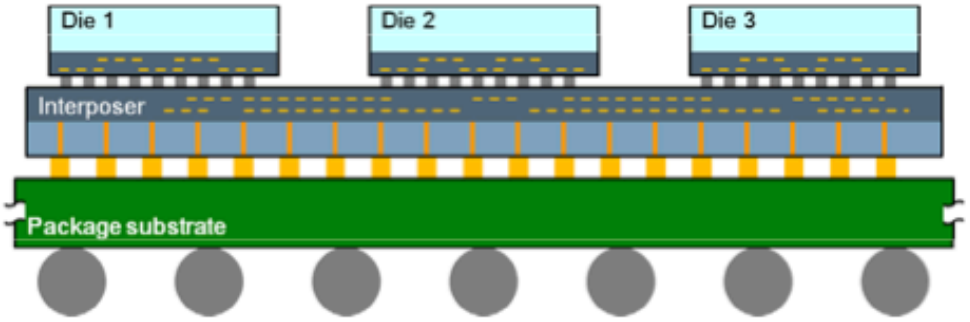
Endless Stacking Opportunities

"Whatever your children can make using Lego bricks"

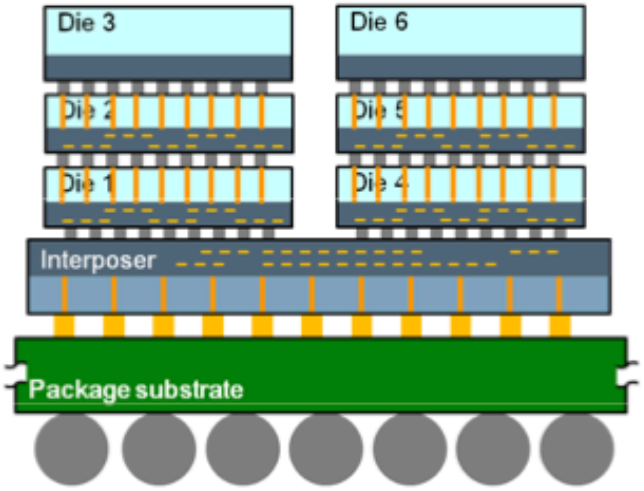
- **3D-SIC**



- **2½D-SIC**

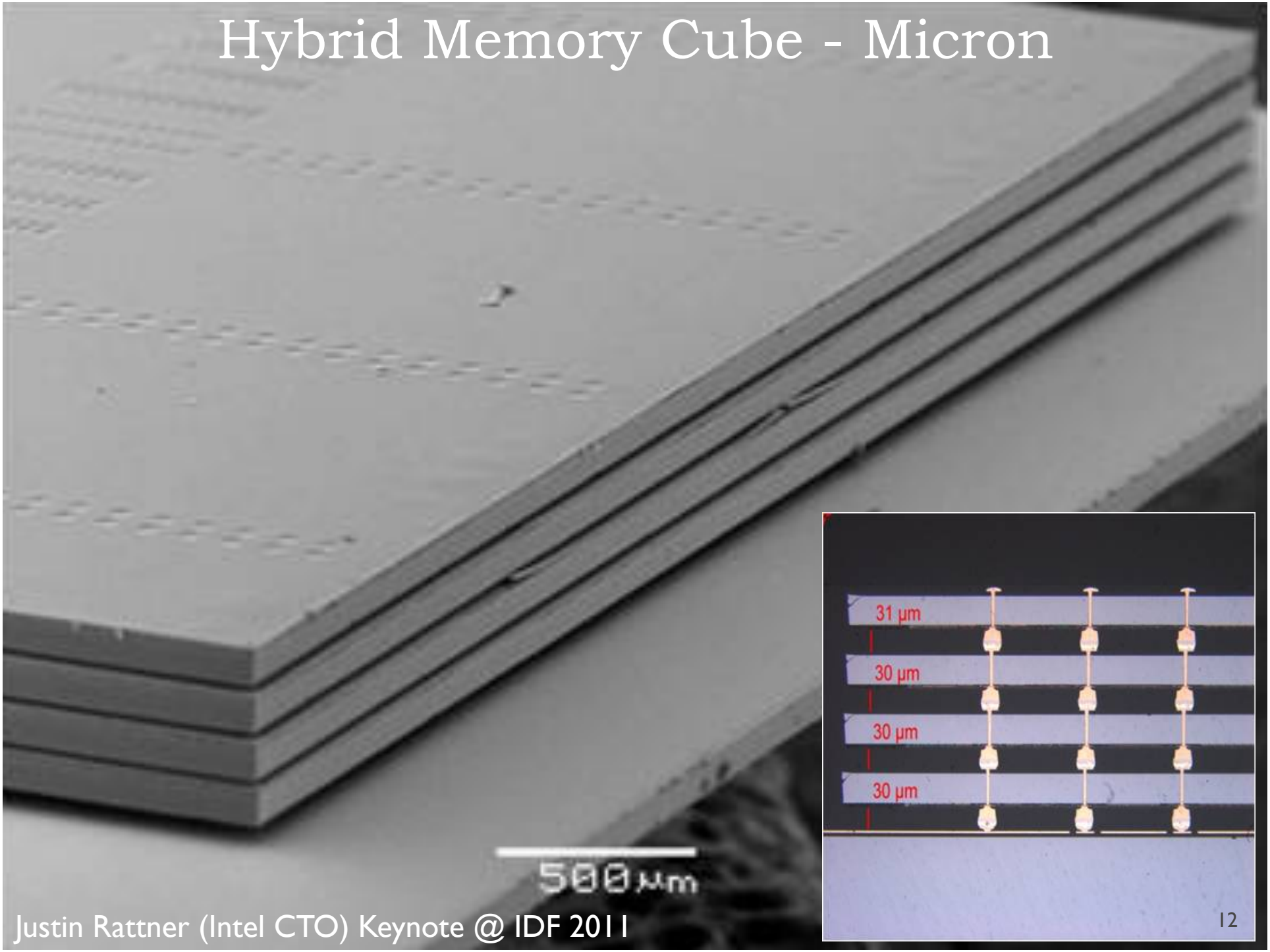


- **2½D + 3D = *5½D-SIC***



"Wafer Probing on Fine-Pitch Micro-Bumps for 2.5D- and 3D-SICs", Erik Jan Marinissen (IMEC), Peter Hanaway (Cascade Microtech), et. al.

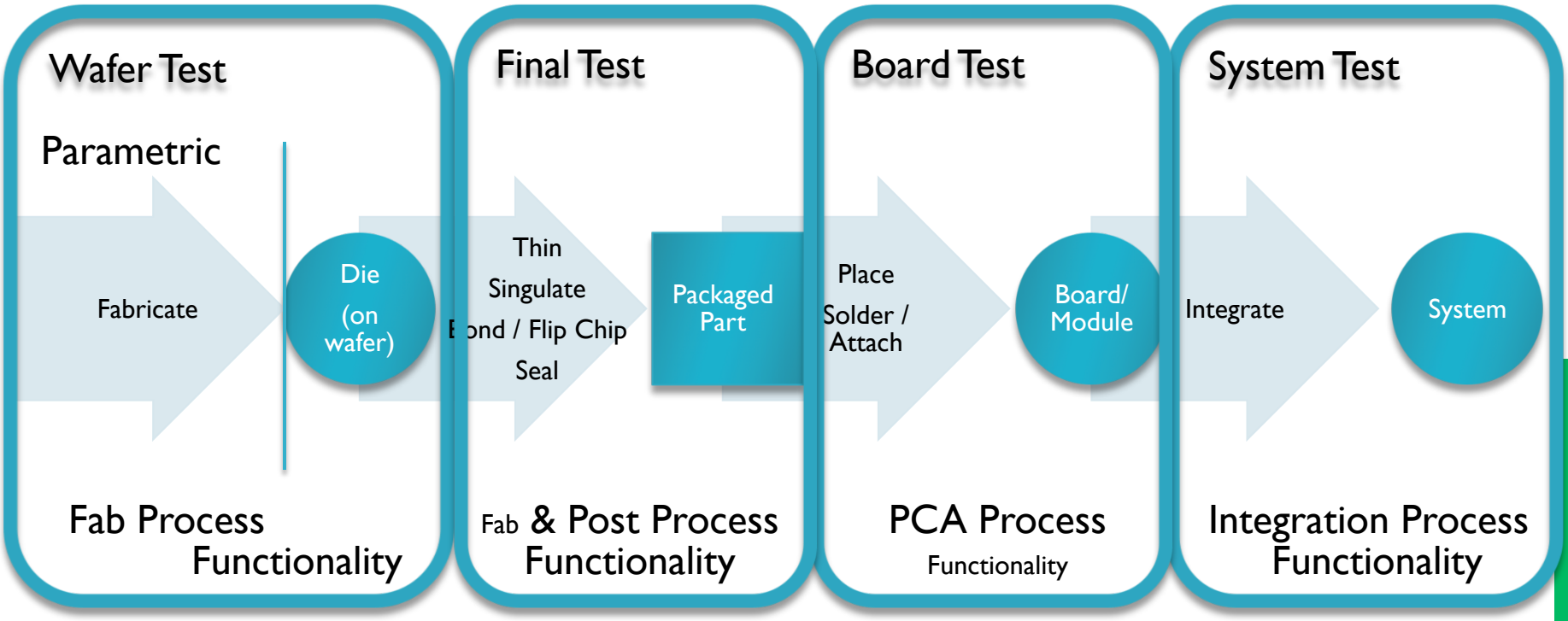
Hybrid Memory Cube - Micron



Justin Rattner (Intel CTO) Keynote @ IDF 2011

Process Flow & Test Coverage

TODAY

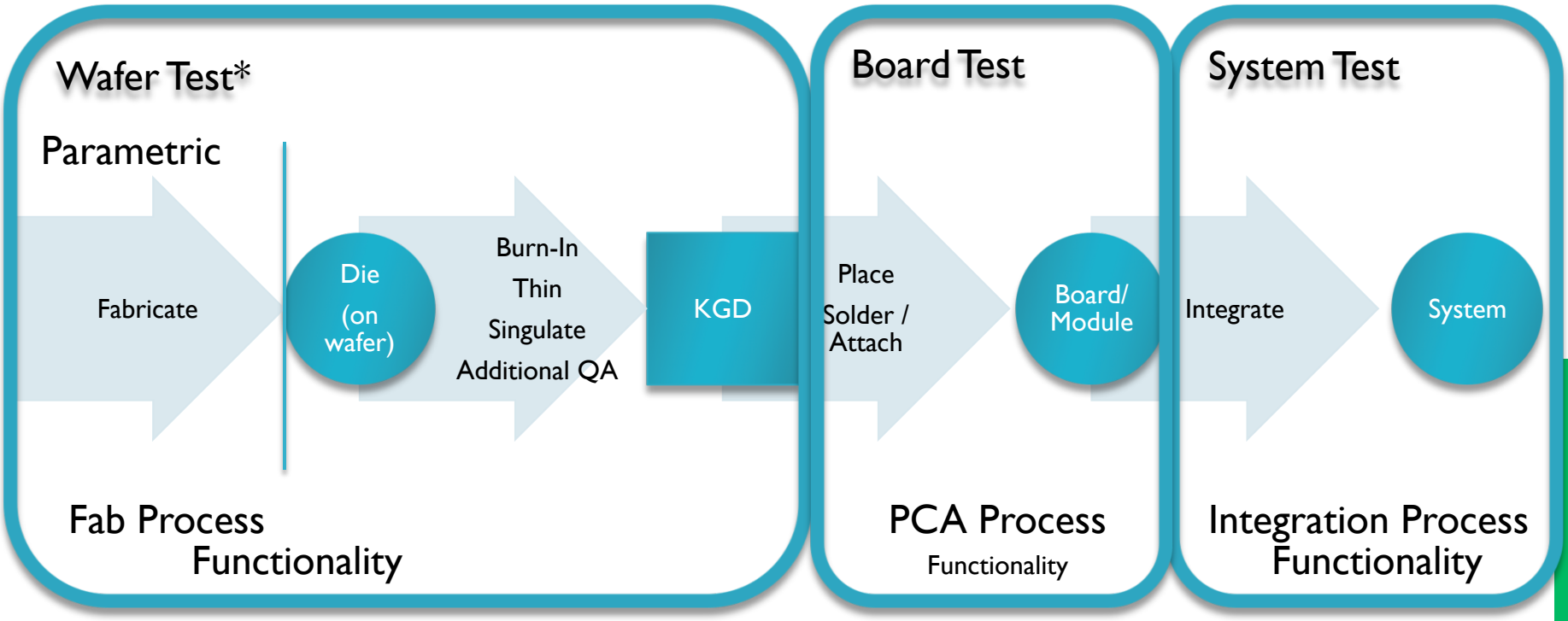


Partial to full speed

At full speed

Known Good Die - Flow & Test Coverage

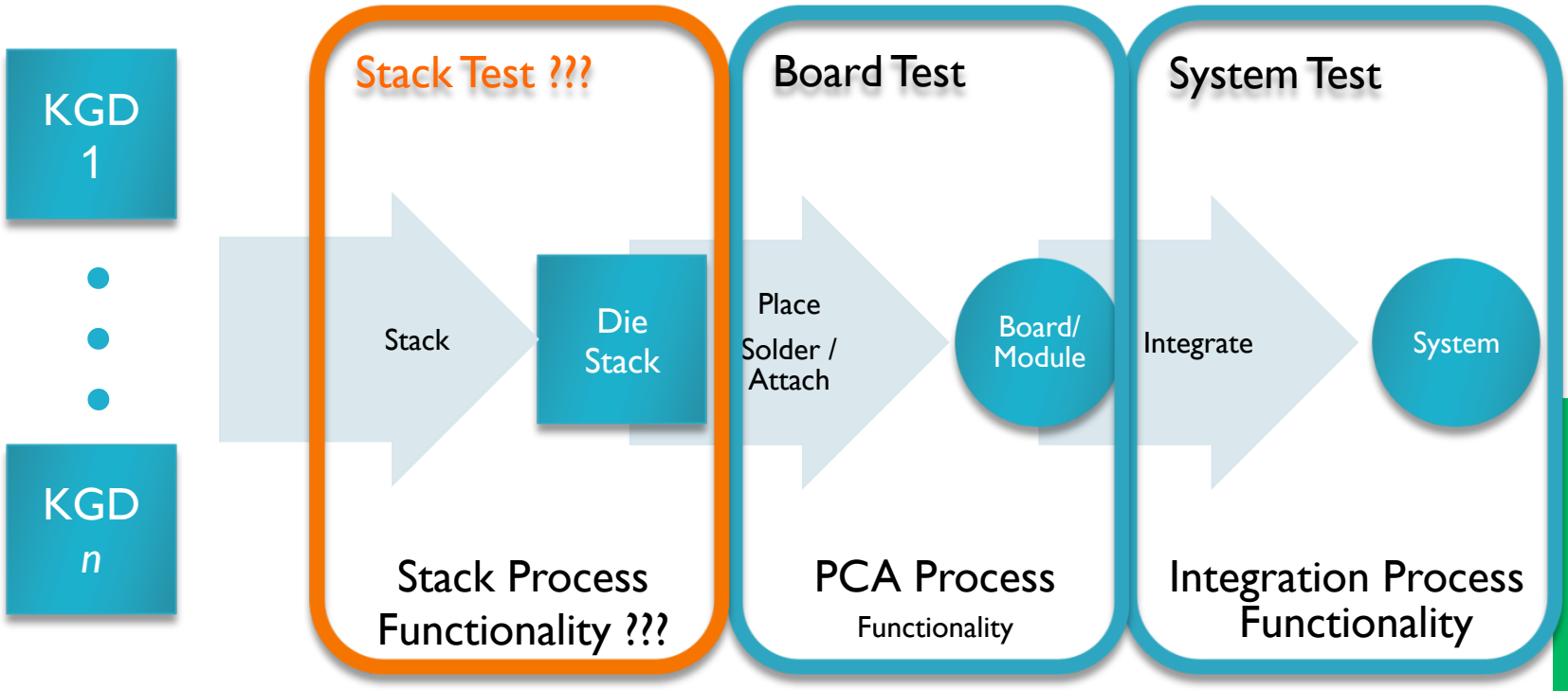
TODAY



At full speed

* Predominant path to KGD is via wafer based testing. There are some solutions for die based socket testing such as Aehr Test's DiePak.

Stacked Die – KGD (singulated)

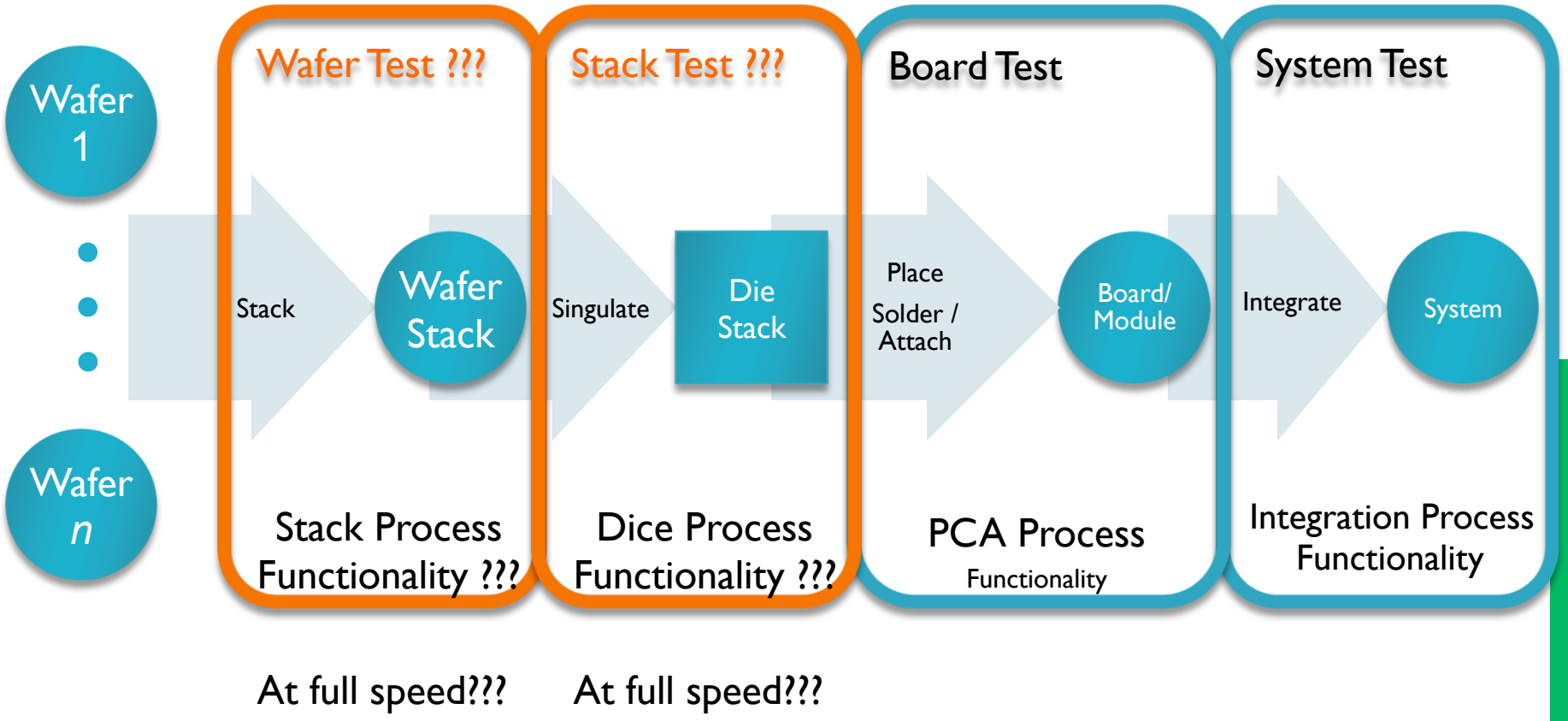


At full speed???

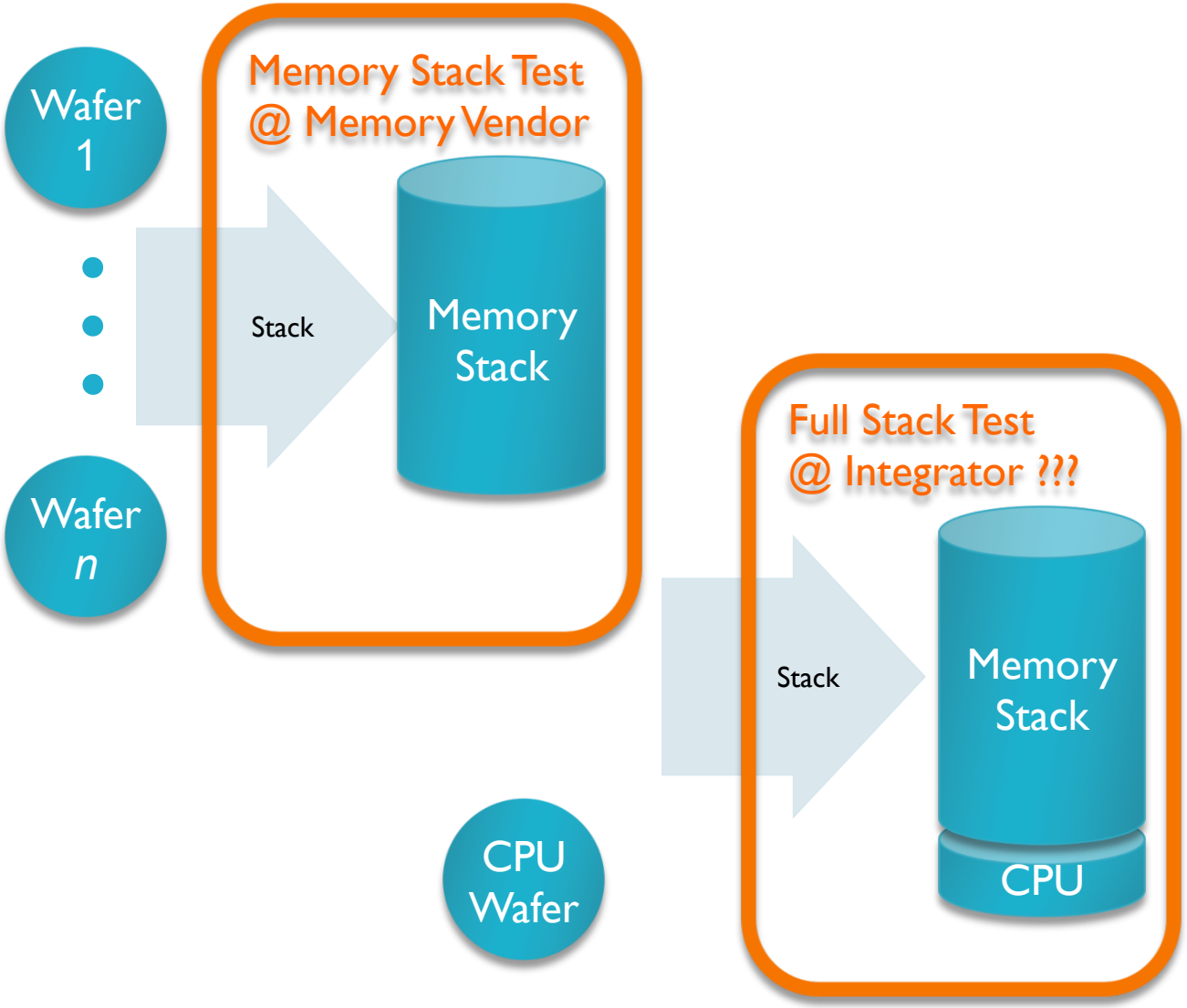
Stacked Die – NKBD (wafers)

Wafers or reconstituted wafers of Not Known Bad Die:

- Thinned
- Partial to full speed tested



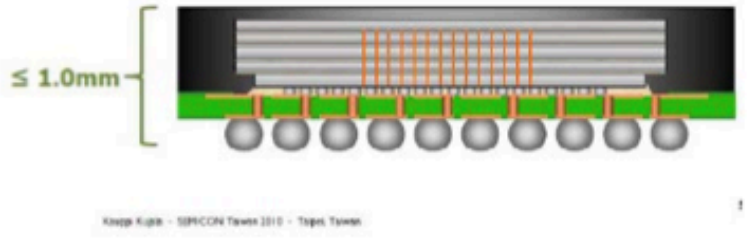
Stacked Die – Sub Stacks (wafers)



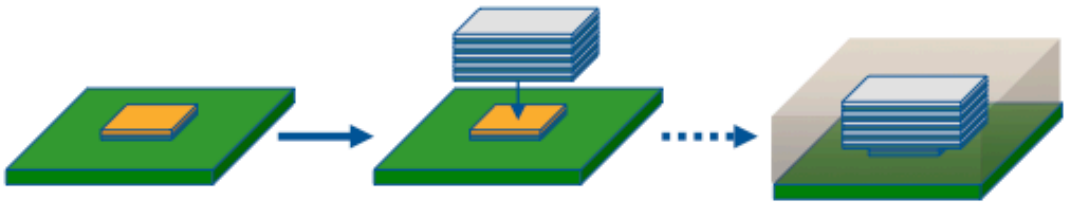
Reference Product / Structure / Flow

SEMATECH

Reference product:
Mobile wide I/O DRAM on logic

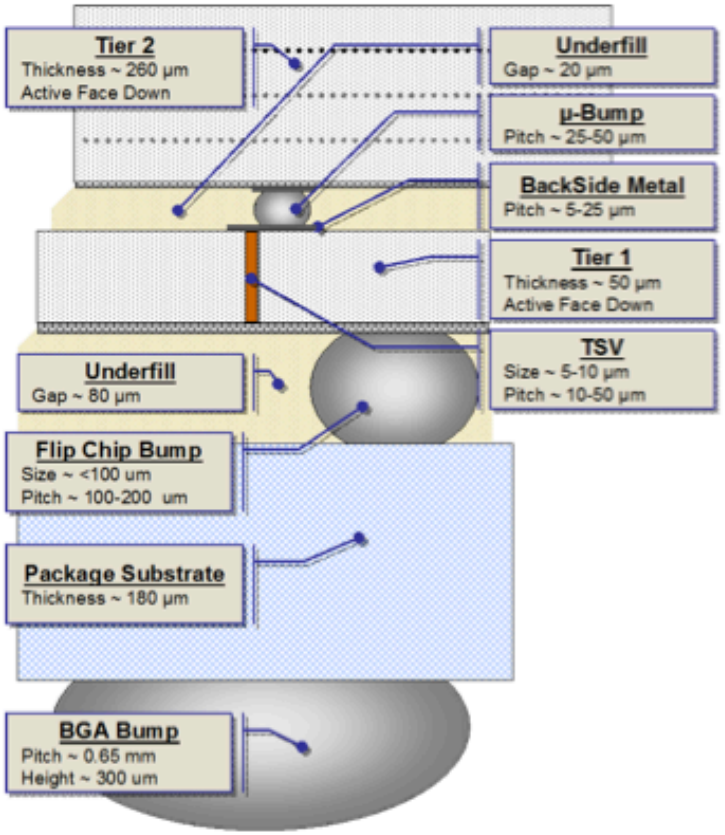


Reference flow candidate



Tier 1 | Tier 2 to Tier 1 die attach | Molding, etc.

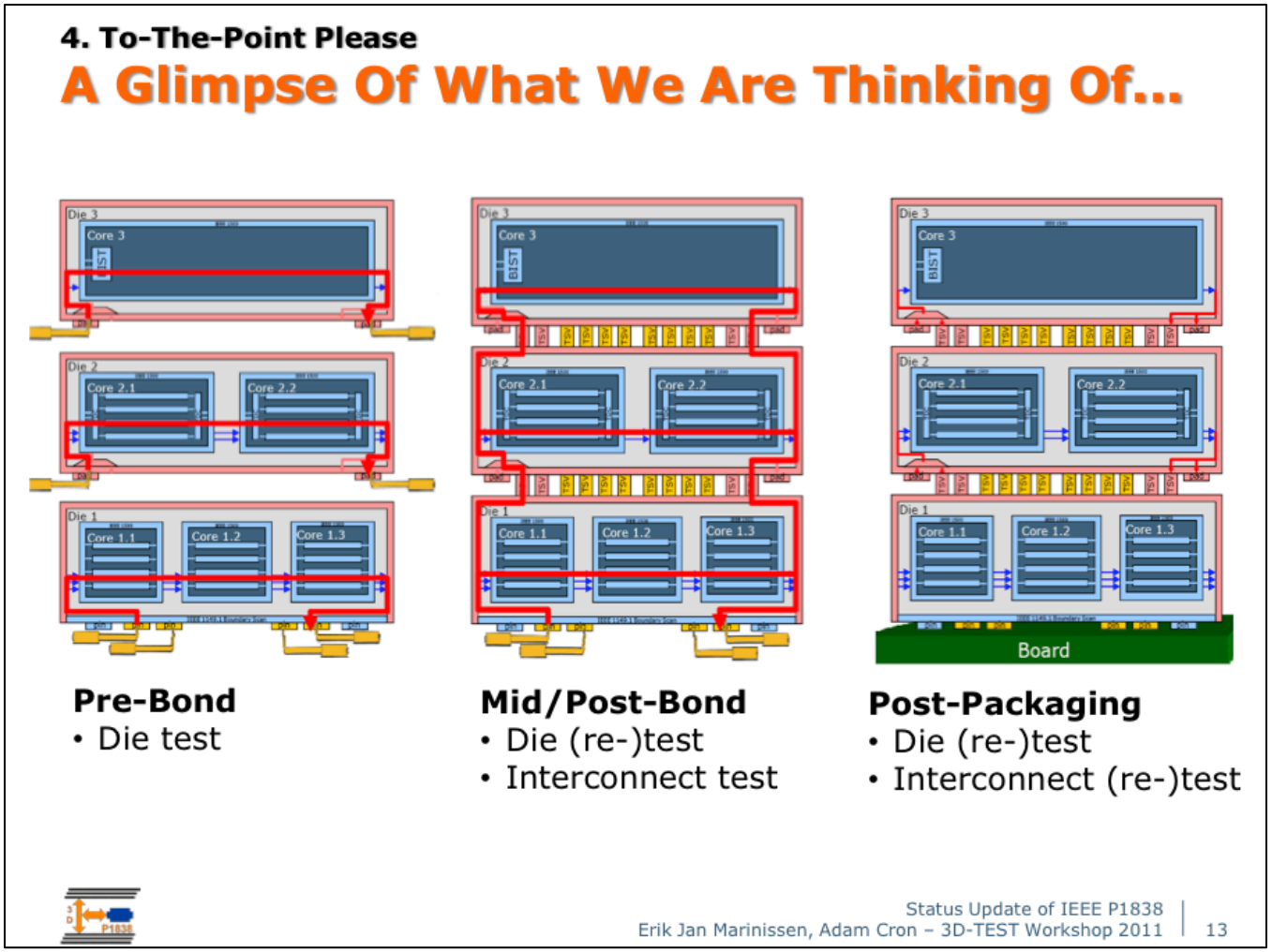
Reference structure



"3D TSV Program Overview – Presented to GSA Oct 20, 2011" Sitaram Arkalgud, SEMATECH

Scan Testing

- Provide access and control to cores at all test steps
  - If proper infrastructure (P1838) & connectivity is present
- Does not replace full access to all "pads" for KGD.



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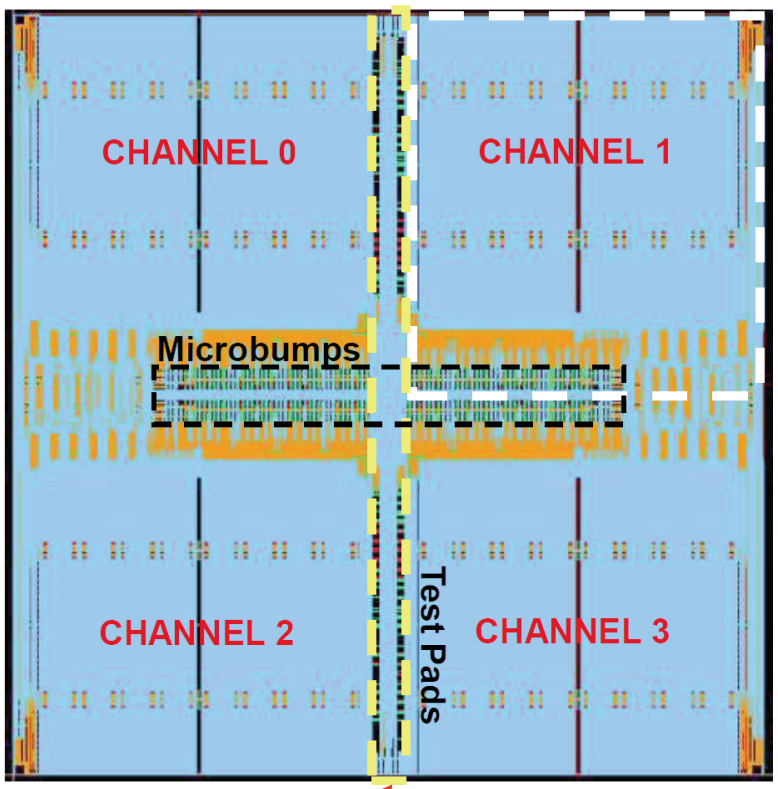
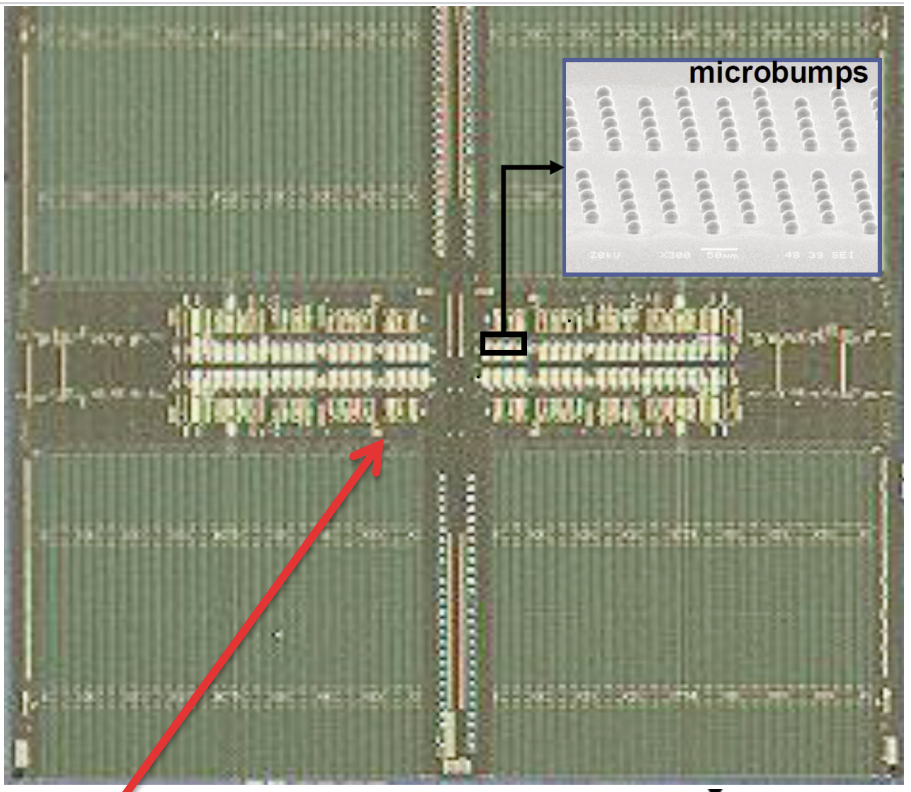
Mobile DRAM predecessor to Wide I/O

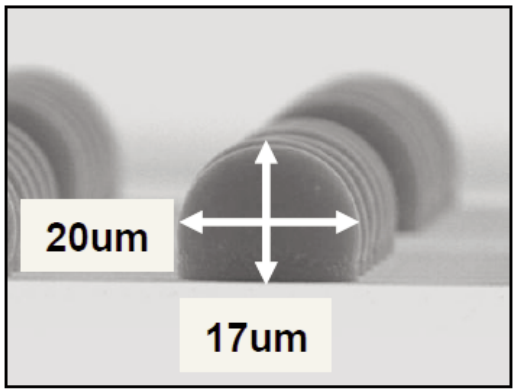


Al pads (muxed) to test with existing probe technology



SEM image of microbumps

> 1000 micro-bumps
50 µm pitch array

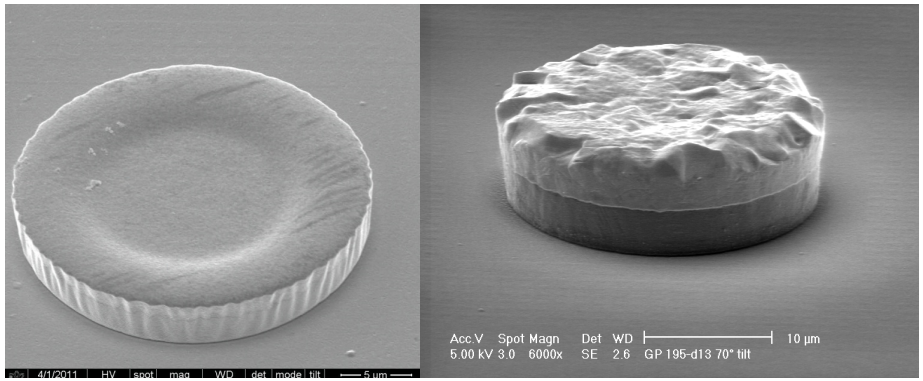


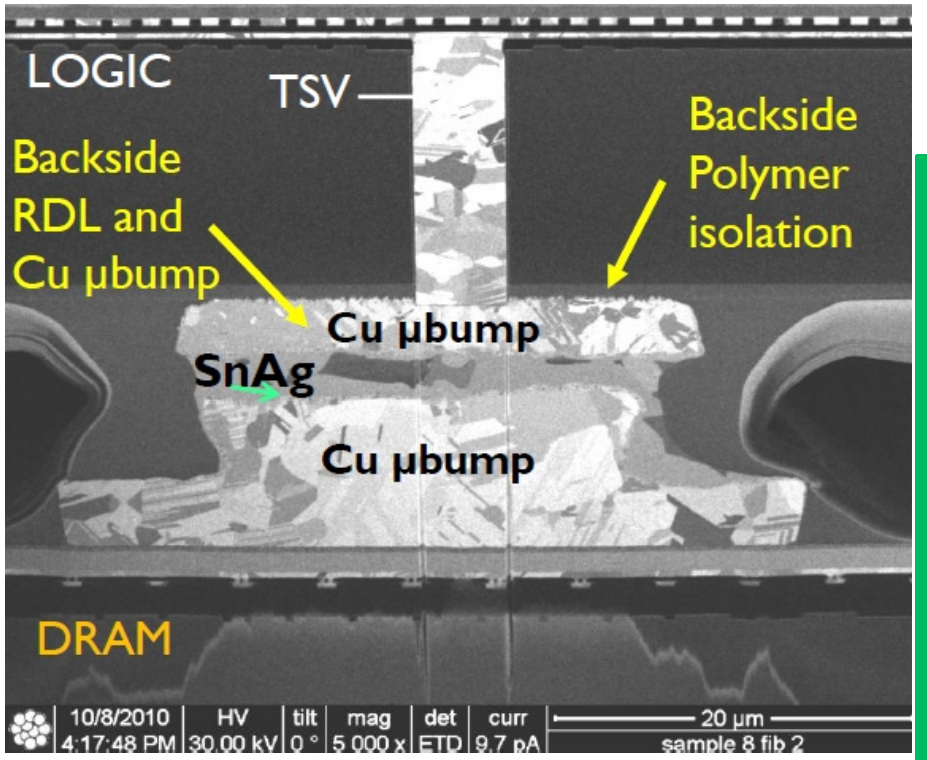
"A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4×128 I/Os Using TSV-Based Stacking" Jung-Sik Kim, et.al., Samsung Electronics, ISSCC 2011

Electroplated Micro-Bump Bonding

- Cylindrical bumps
  - Side1: Cu (5 µm)
  - Side2: CuSn (5 µm + 3.5 µm)

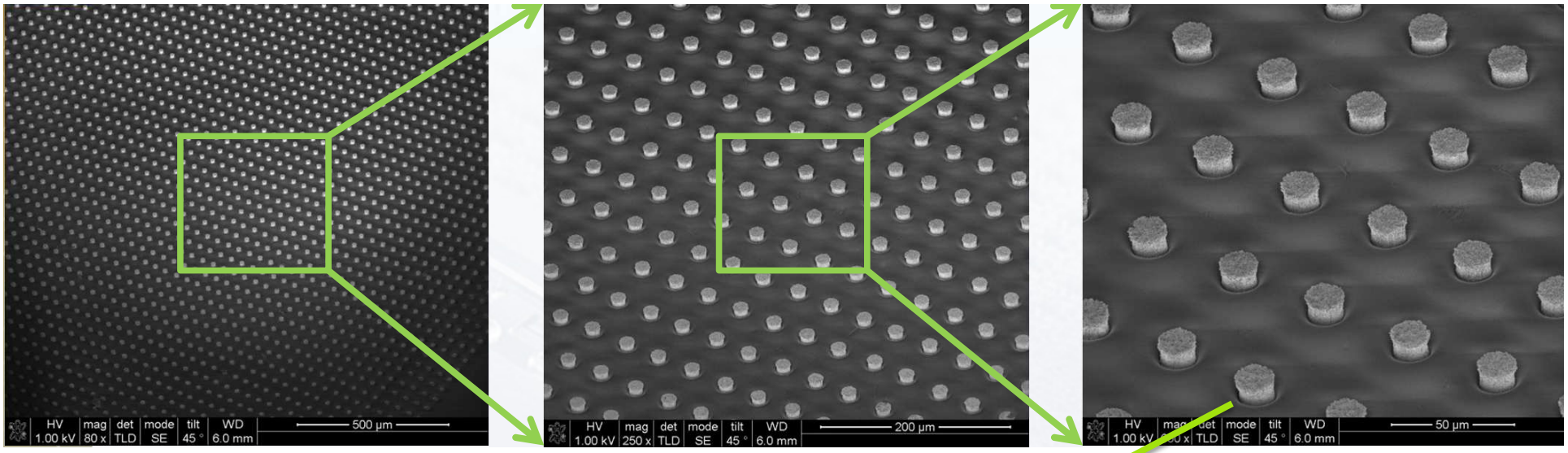
- Size (today)
  - Diameter : 25 µm
  - Pitch : 40 µm
  - Scaling down…



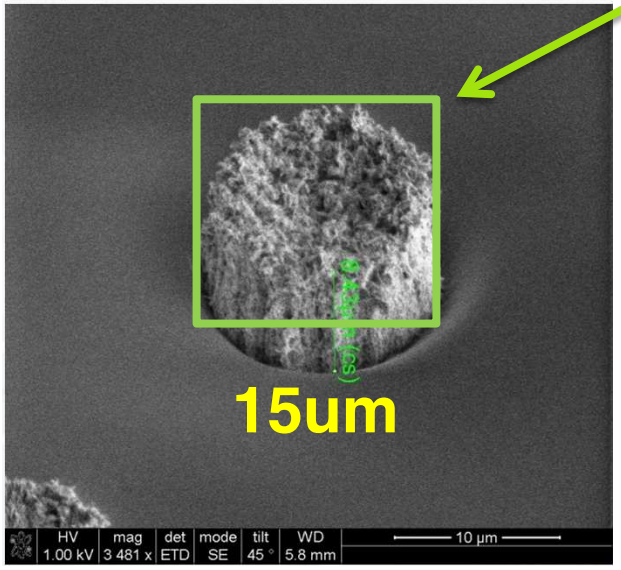


Courtesy of Cascade Microtech & IMEC

FormFactor: NanoPierce Contact

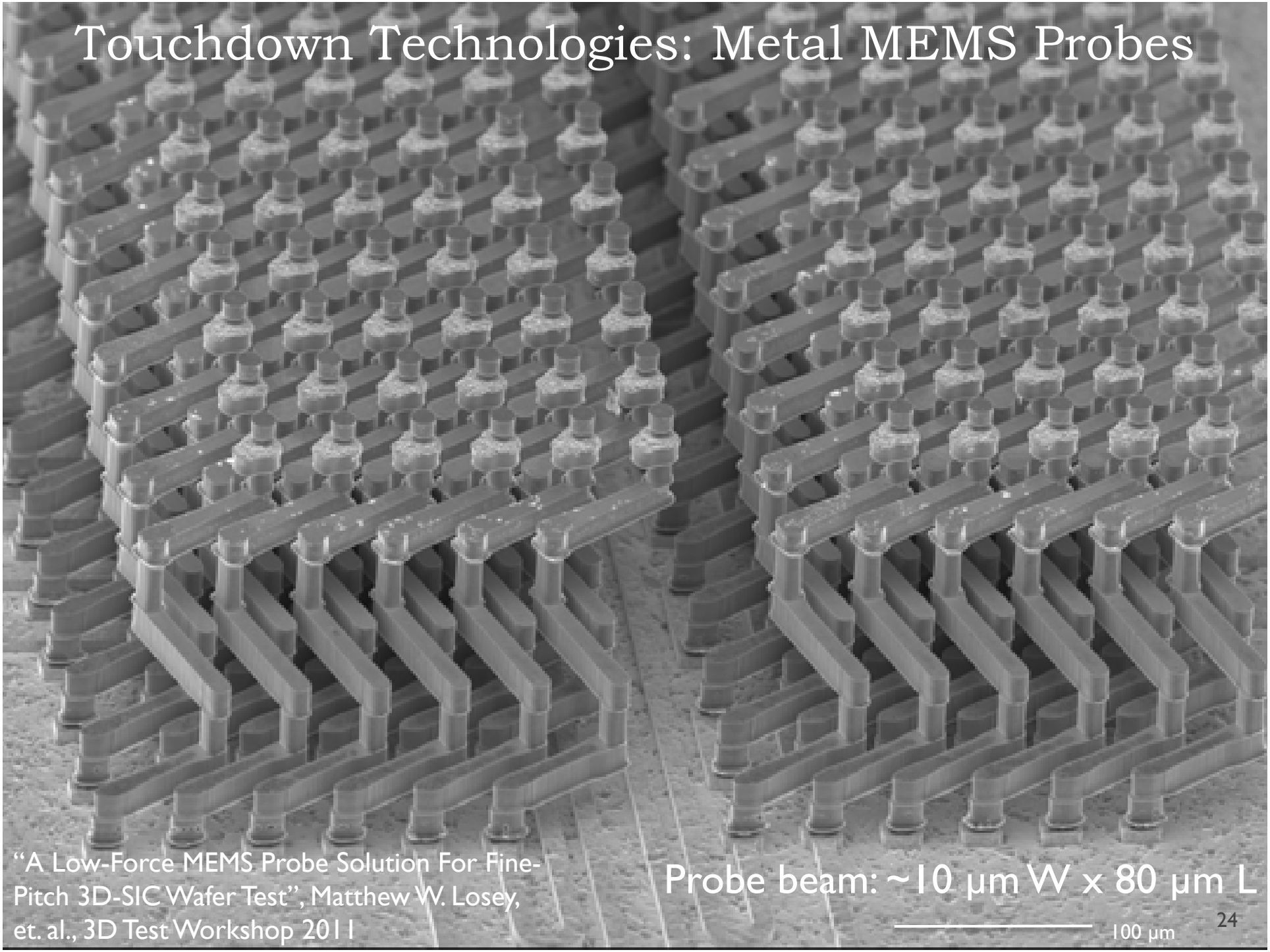


Metal "NanoFiber" contact element



"Challenges and Solutions for Testing of TSV and MicroBump Devices by Direct Connection", Ben Eldridge, 3D Test Workshop 2011

Touchdown Technologies: Metal MEMS Probes

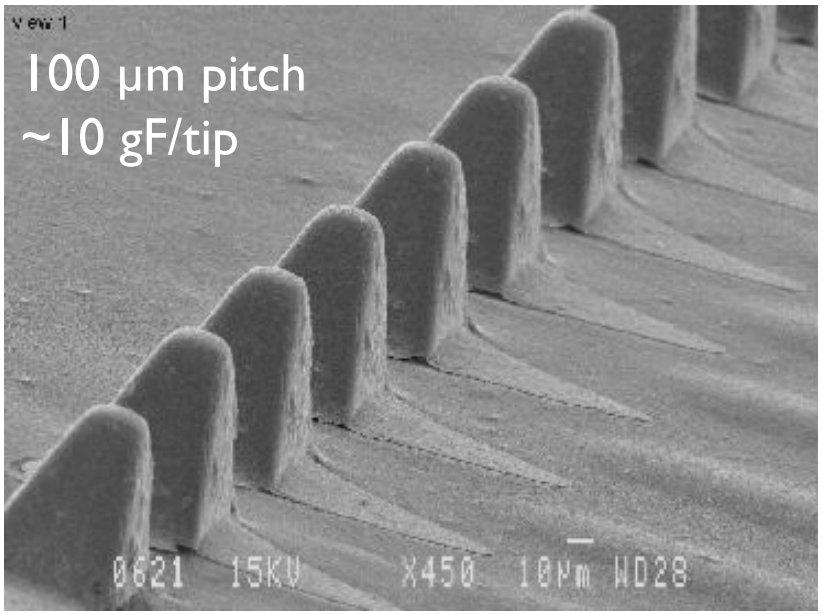


"A Low-Force MEMS Probe Solution For Fine-Pitch 3D-SIC Wafer Test", Matthew W. Losey, et. al., 3D Test Workshop 2011

Probe beam: ~10 µm W x 80 µm L

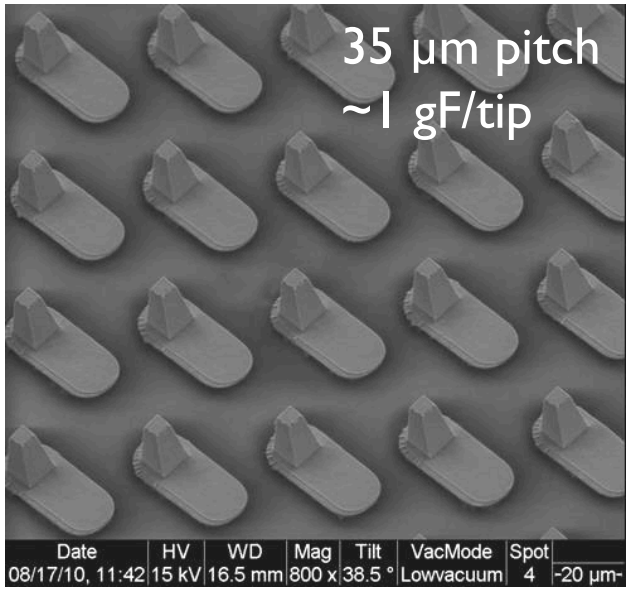
100 µm

Cascade Microtech: Lithographically Printed

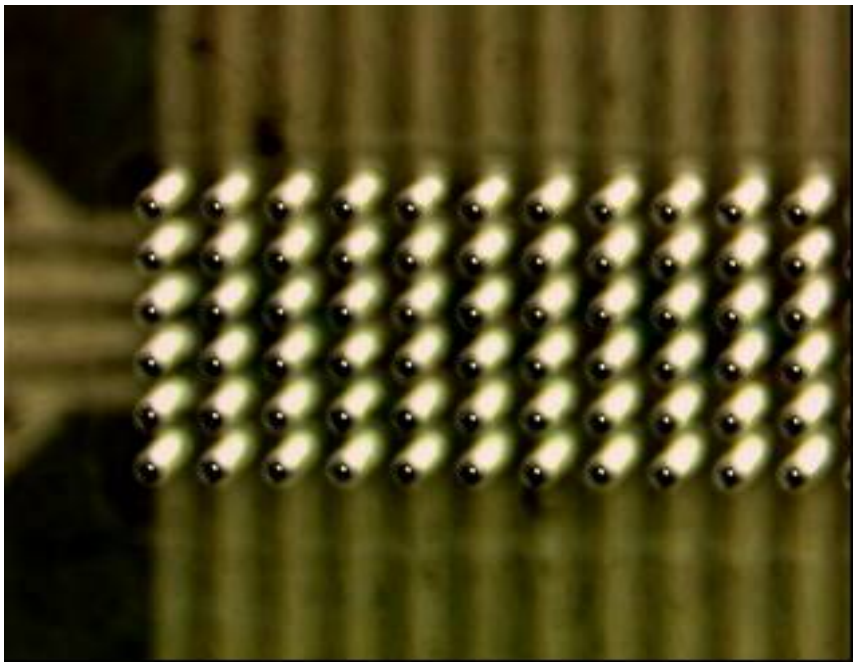


Scale by K

XYZ/K
Force/K²



Fully-routed 6 x 50 array at 40 x 50 µm pitch
New space transformer technology



"Probing Strategies for Through-Silicon Stacking",
Eric Strid, et. al, 3D Test Workshop 2011

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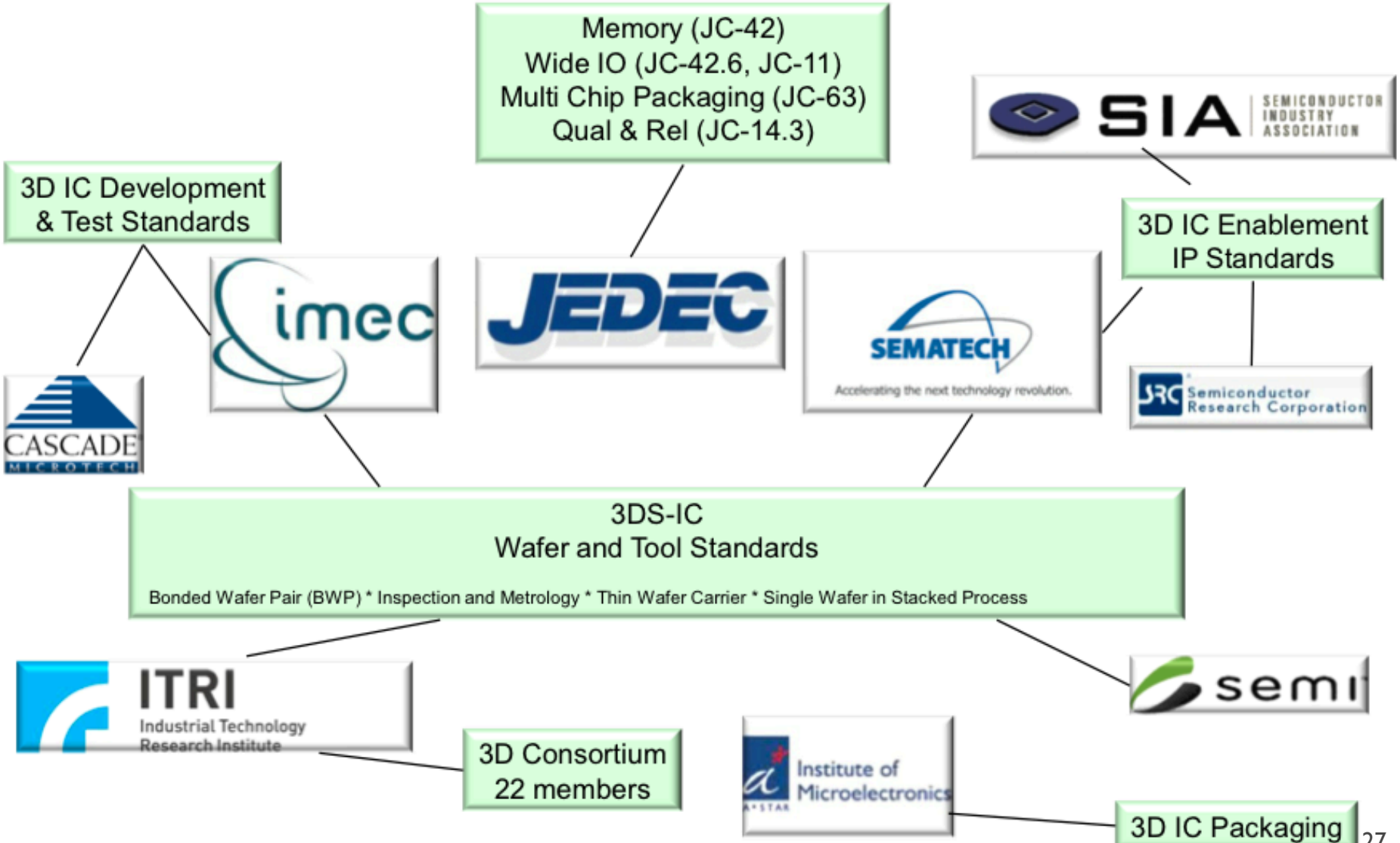
Developing Eco-system Standards and Clusters



[37]"3D IC Technology's Promise for Communications and Storage ICs", Brian D. Gerson, PMC-Sierra, GSA 4/28/11

Organizations & Programs

- IEEE P1838 - Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits standards.ieee.org/develop/project/1838.html
- Semi wiki.sematech.org/3D-Standards
- Sematech – 3D Program www.sematech.org/research/3D
  - Unit Process, Module Development, Enablement Center
- Global Semiconductor Alliance – 3D-IC Working Group www.gsaglobal.org/3dic
- JEDEC – Wide I/O www.jedec.org
- IMEC www2.imec.be
- Industrial Technology Research Institute (ITRI) www.itri.org.tw
- A*Star Institute of Microelectronics www.ime.a-star.edu.sg

Recent Conferences

- GSA Memory Conference (Mar '11) www.gsaglobal.org/events/2011/0331/program.aspx
- IEEE Semiconductor Wafer Test Workshop (June '11 & '12) www.swtest.org
- ATE Vision 2020 (w/Semicon West – Jul '11) www.atevision.com
- Semicon Taiwan – SiP Global Summit 2011 (Sep '11)
  - 3D IC Test Forum semicontaiwan.org/en/node/1566
  - 3D IC Technology Forum semicontaiwan.org/en/node/1571
- IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (w/ITC – Sep '11 / Nov '12) 3dtest.tttc-events.org
- MEPTEC 2.5D, 3D and Beyond – Bringing 3D Integration to the Packaging Mainstream (Nov 9, 11) www.meptec.org
- MEPTEC-Semi KGD in an Era of Multi-Die Packaging and 3D Integration (Nov 10, 11) www.meptec.org

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TBD - To Be Determined

- Yield
- Preferred Via Process
- Singulate dies before or after stacking
- Wafer probe and handling of die stacks on wafer or singulated stacks
- Business models – who is responsible for what

Future

Profits or Costs?

- Hard work – getting it to work!
- Increased test complexity earlier in process
- Shrinks – especially micro-bumps and pitch

Thank You!

Ira Feldman
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Visit my blog
www.hightechbizdev.com
for additional resources.

Other References & Resources

- Hybrid Memory Cube Consortium www.hybridmemorycube.org
- 3D-IC Alliance www.3d-ic.org (event & blogs/paper listing)

- Discussion groups / 3D news:
  - www.3dincites.com
  - www.3d-ics.com
  - 3D-IC group on www.linkedin.com