## Feldman Engineering

# Semiconductor Wafer Test Technology and Trends: Lessons for MEMS Test Engineers

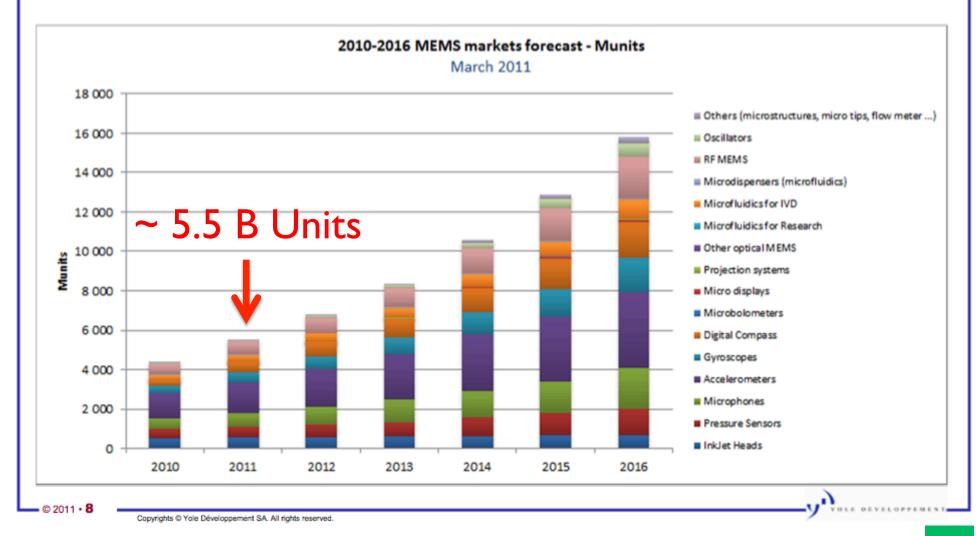
Ira Feldman October 20, 2011

### Outline

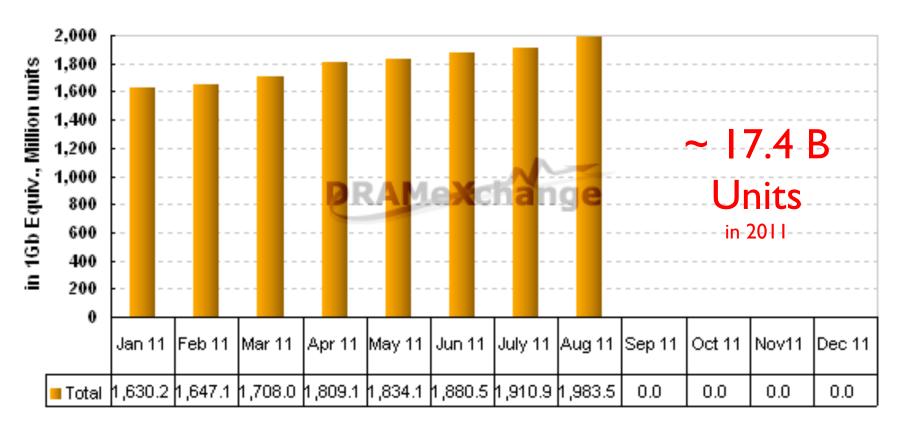
- Market Dynamics
- Testing Semiconductors vs. MEMS
- Cost of Test
  - Semiconductor Solutions
- MEMS Challenges
- MEMS @ Semiconductor Wafer Test Workshop
- Conclusion

# NEW 2011 Yole MEMS Forecasts In units

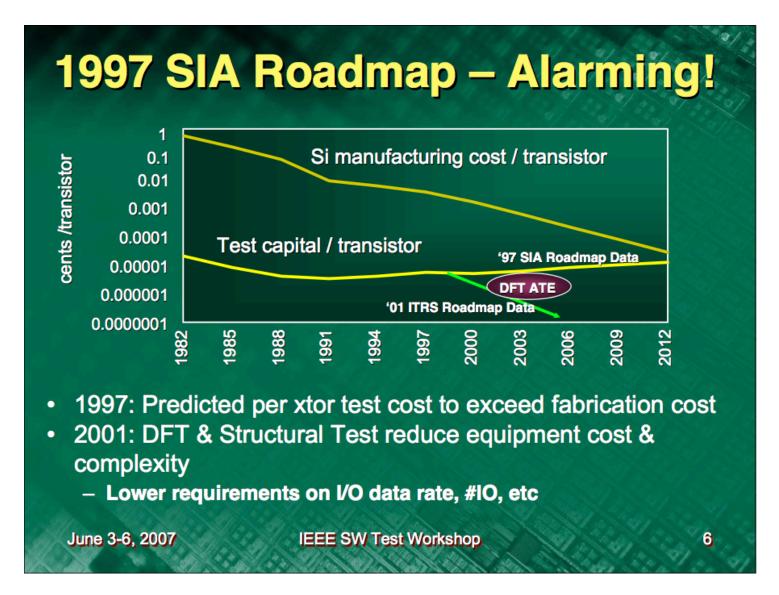
15.8 Bunits of MEMS devices in 2016 with a 24% CAGR over 2010-2016



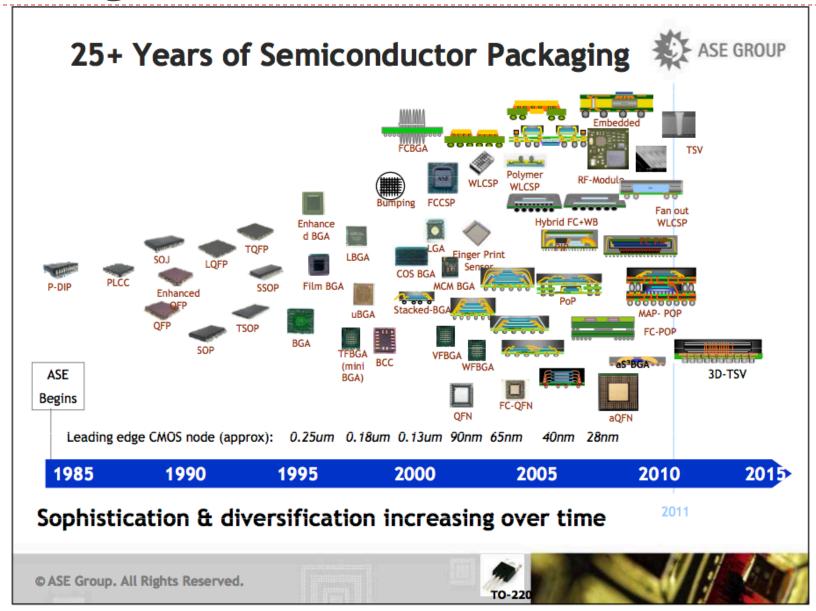
#### Worldwide Production in 2011



### Cost of Test - Constant Pressure



# Package Proliferation

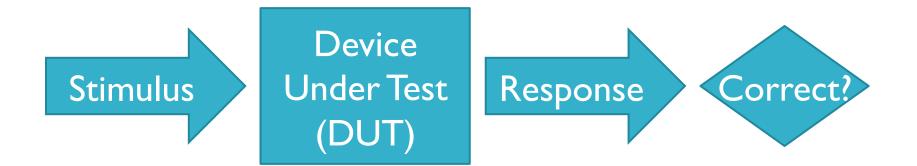


"Backend to the Front Line" William Chen, ASE Group, SWTW 2011

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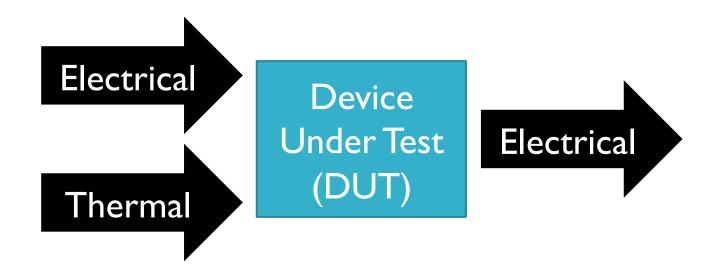
# Device Testing



### Traditional Wafer Probe Test Cell

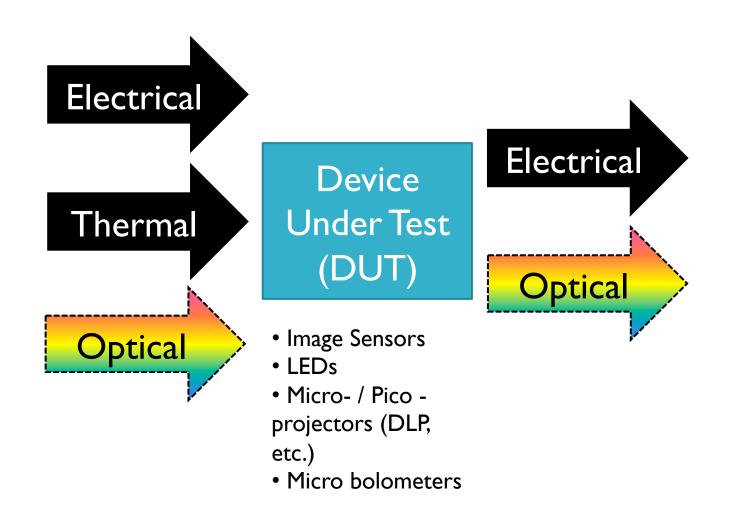


# Stimulus & Response - Traditional

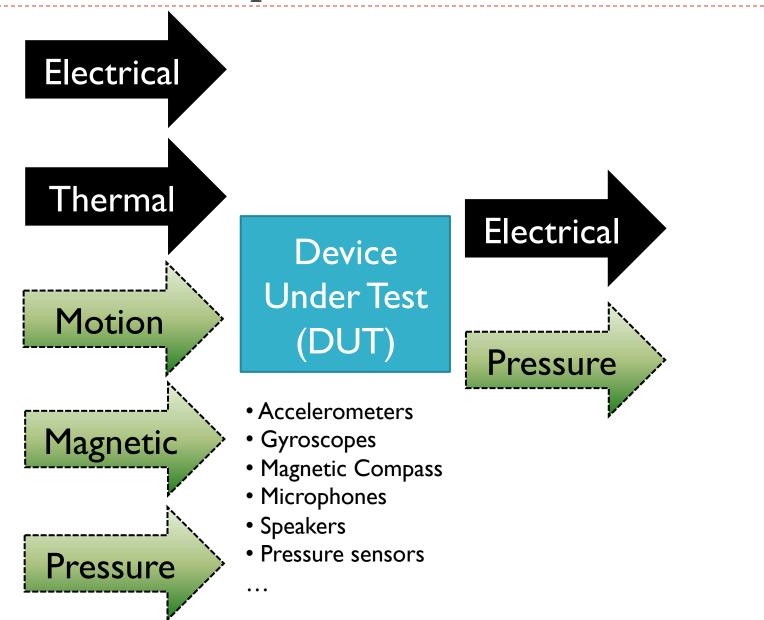


- Semiconductors
- Oscillators
- MEMS switches
- MEMS filters
- MEMS oscillators

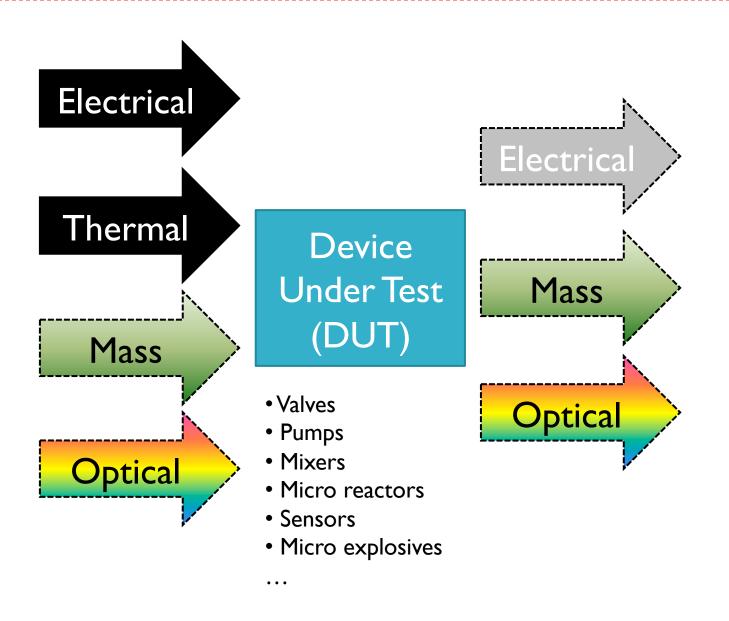
# Stimulus & Response - Optical



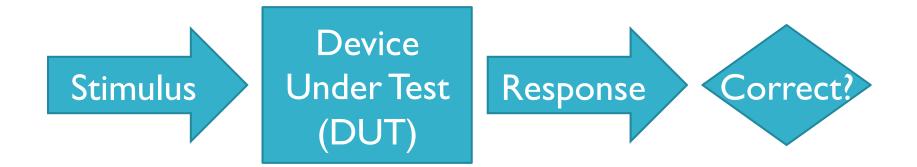
# Stimulus & Response – MEMS Sensors



# Stimulus & Response – Life Science +?



# Device Testing



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### Cost of Test Drivers

Increasing test frequency

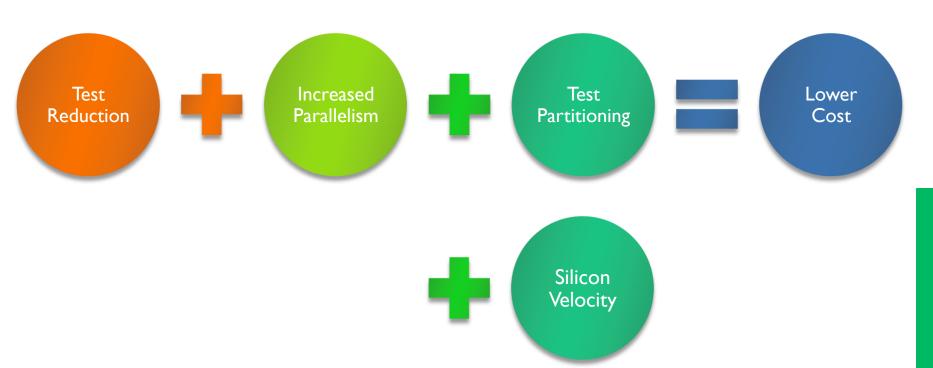
Tighter pad pitches

Increasing transistor count

Increased Cost

Increasing probe count

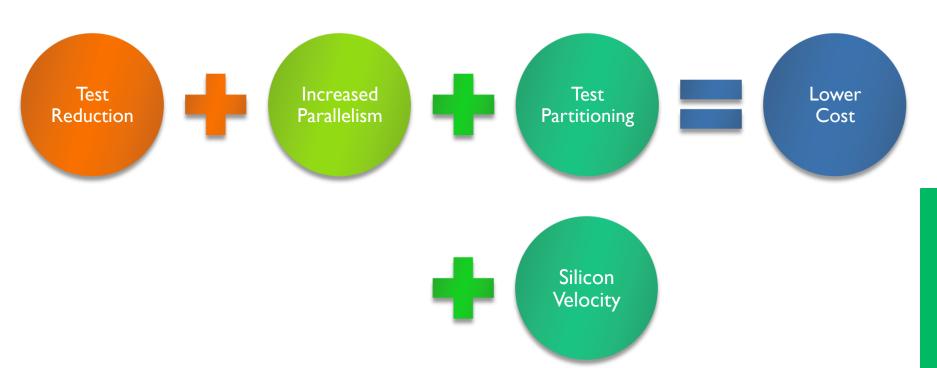
### Semiconductor Cost - Test Solutions





MEMS Testing & Reliability Conference 2011

### Semiconductor Cost - Test Solutions





- Test Escapes
- Run time complexity
- + Statistical based sampling
- + Test elimination



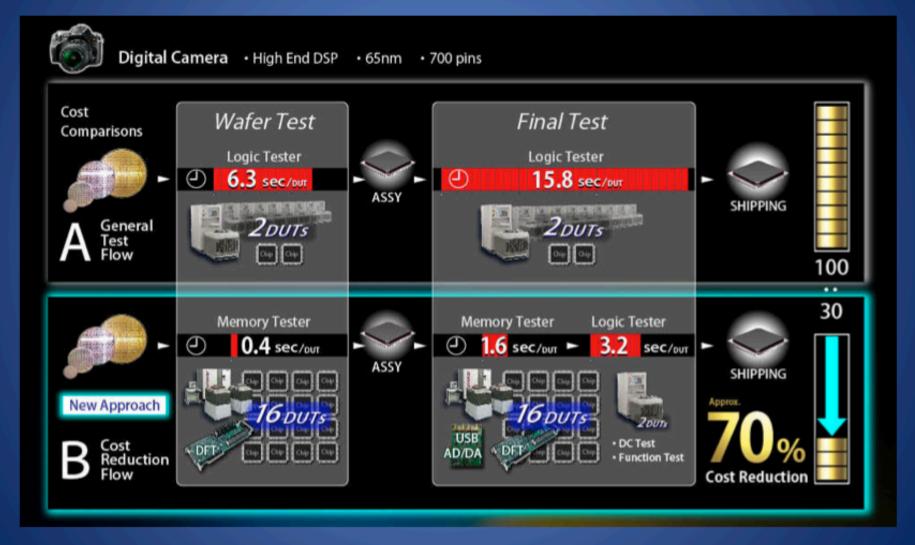
- Increased probe card cost
- Increased tester resources
- + Decreased handling time
- + Greater prober amortization
- + Reduced floor space
- + Increased Silicon Velocity



- Increased process steps
- Increased process complexity
- + Optimized high-cost ATE

# Remo

#### Example of using old depreciated Memory Testers to Reduce Test Costs

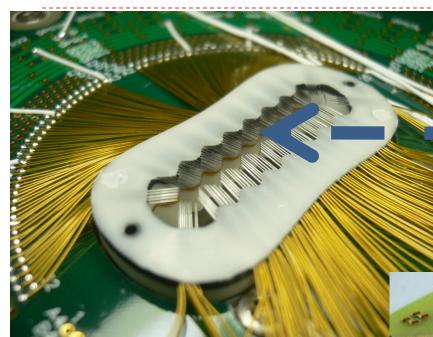


### Outline

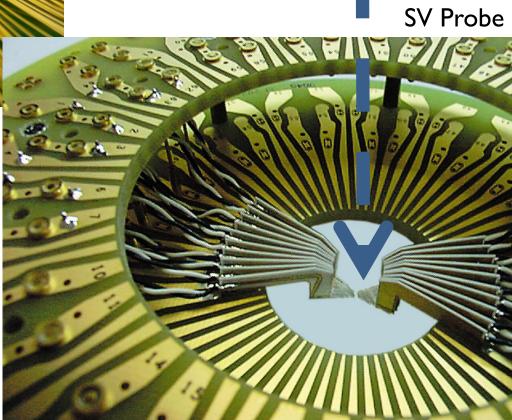
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# Cantilever & Blade

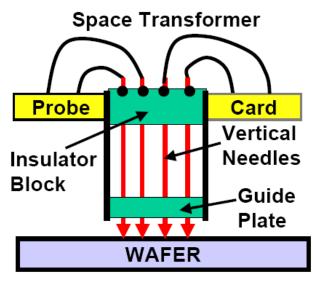


Technoprobe





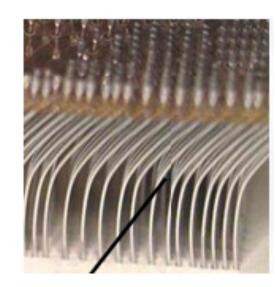
# Vertical - Buckling Beam



Cobra "Buckling Beam" Card Patented by IBM in June 1977

Mann: SWTW Tutorial 2004



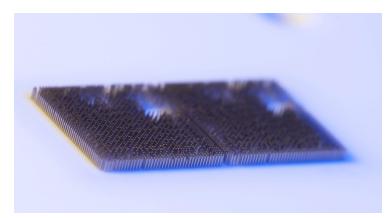


FormFactor: "MEMS for ProbeCard Applications" Chong Chan Pin – Semicon Singapore 2010

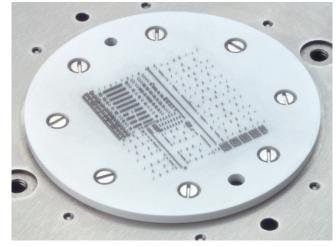


JEM "VC"

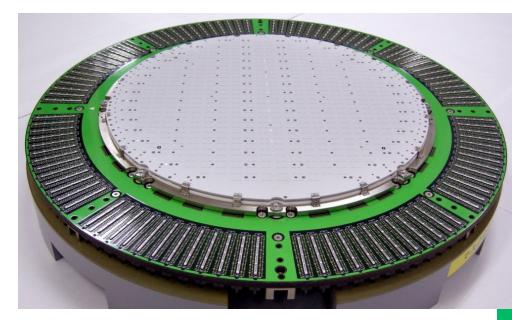
# Vertical - Buckling Beam



MicroProbe: Apollo Vertical

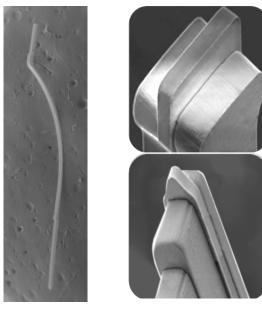


SV Probe:Trio

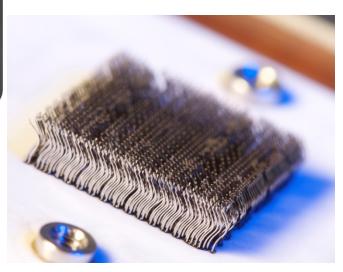


JEM:VC

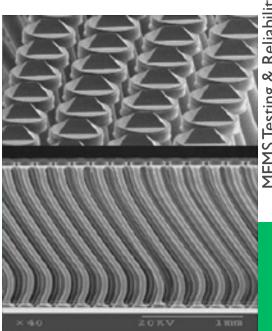
# MEMS - Vertical



Microfabrica MicroProbe

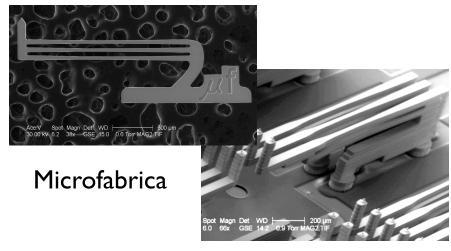


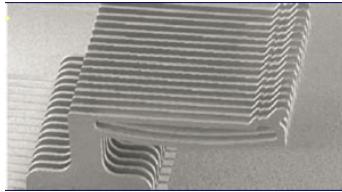
MicroProbe (Vx-MP)



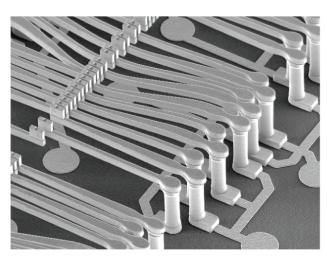
FormFactor (T1)

### MEMS - Micro Cantilever

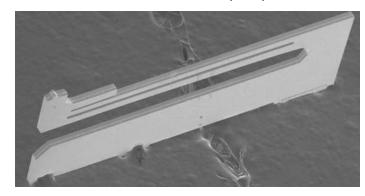




MJC (U Probe)
http://www.mjc.co.jp/eng/ir/pdf/MJC070226-s.pdf

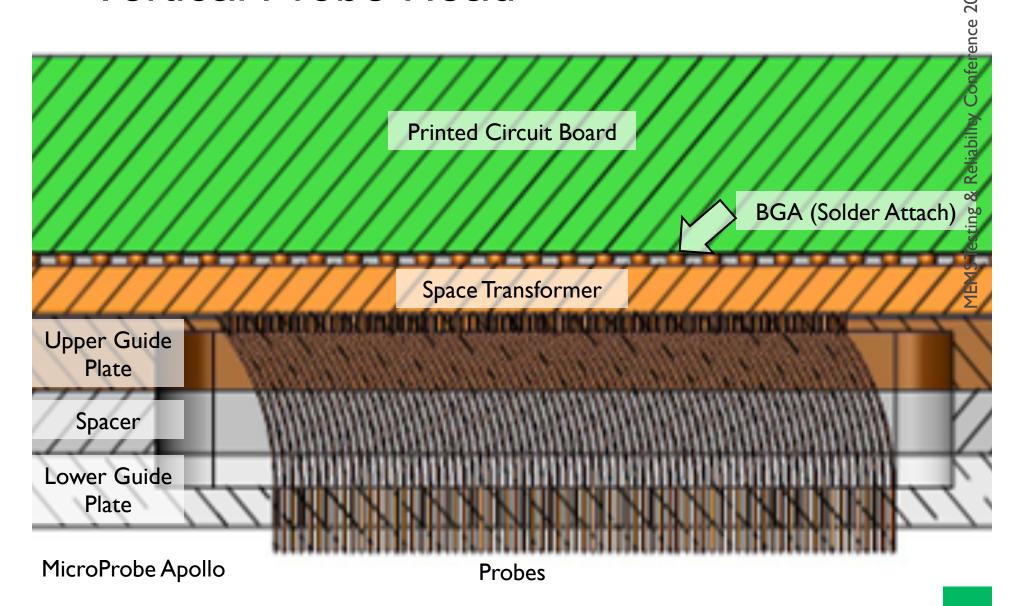


FormFactor (T3)

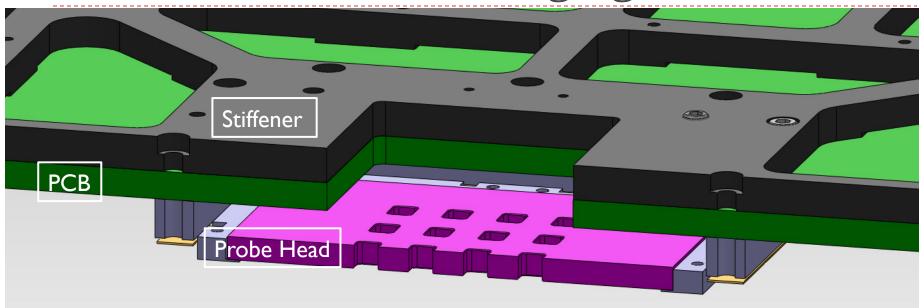


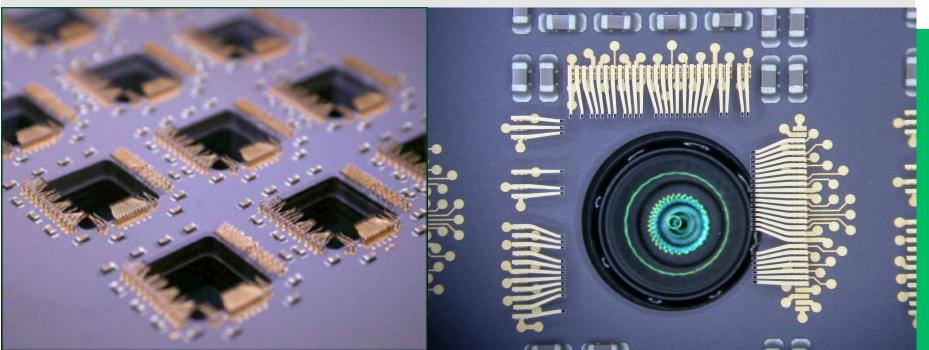
JEM

# **Vertical Probe Head**



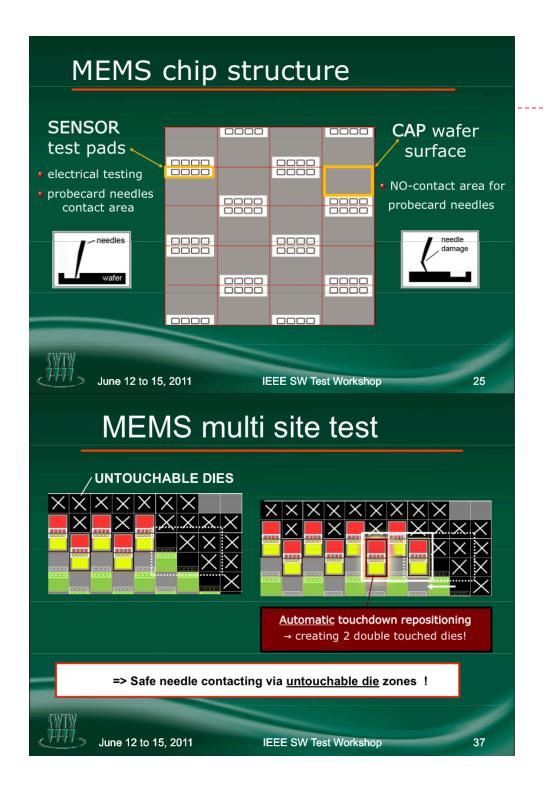
# FormFactor CMOS Imaging Solution





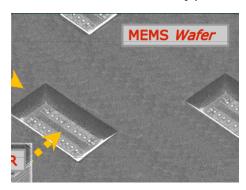
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### SWTW 2011

"MSO - Multi-Site Optimizer" Kevin Fredriken (SPA GmbH - Germany)



- MEMS device alternating rotation across wafer > required two probe passes.
- No probe of cap or wafer exclusion zone
- Developed four site probe card and stepping algorithm using MSO. Inclusive probing with multi-probes on some die.

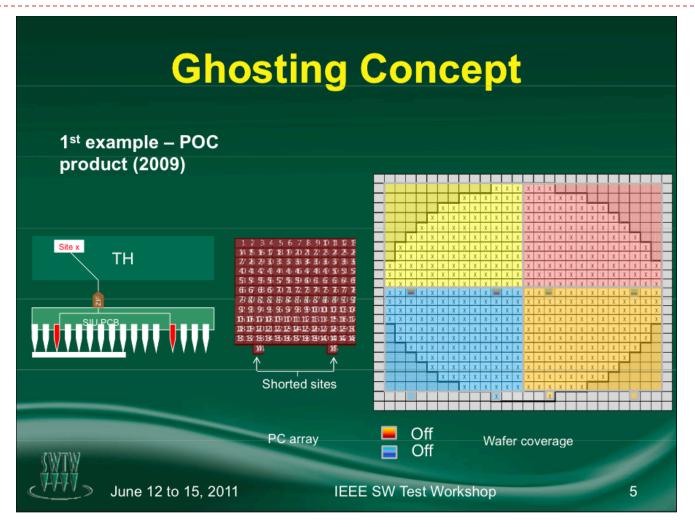
#### Film Bulk Acoustic Resonator New product development geared towards using FBARs in oscillators for timing solutions 1.5GHz resonant frequency Pads •27,000 um<sup>2</sup> resonator area Quality factor over 1000, up to several thousand •1 year aging spec less than 25ppm June 12 to 15, 2011 **De-embedding Structure** Layout Start with Device Under Test (DUT), then reproduce pads replacing device with Open and Device pads Short at device plane Open and Short structure repeated 80 times equally spaced on wafer Open structure June 12 to 15, 2011 IEEE SW Test Workshop

### SWTW 2011

"Probe to Pad Placement Error Correction for Wafer Level S-Parameter Measurements" Steven Ortiz (Avago Technologies - USA)

- FBAR structure resonator plus cap wafer. Vias through cap wafer to resonator.
- Due to very high frequency and tight specification tolerance, very sensitive to location of probes on pad. → Implemented "calibration" structures to deembed the measurements.

### SWTW 2011



"Ghosting - Touchdown Reduction Using Alternate Site Sharing"
Doron Avidar and Yossi Dadi (Micron - Israel)

When using large multisite arrays that need > 3 touchdowns / wafer, "ghosting" may save several touchdowns. Examples showed I 2 to 20% savings.

# Summary

- Proven semiconductor cost reduction techniques
  - Not always intuitive
  - Require test engineering
  - Can be applied to MEMS
- MEMS wafer test challenge
  - Multi-site stimulus and response
  - Proper probe card architectures required
  - Solution integration support

### Resources

- ▶ IEEE Semiconductor Wafer Test Workshop (SWTW)
  - http://www.swtest.org
- International SEMATECH Manufacturing Initiative (ISMI) Probe Card Cost Model
  - http://ismi.sematech.org/modeling/probeCOO.htm
- SEMI E35-0307
  - Guide to Calculate Cost of Ownership (COO) Metrics for Semiconductor Manufacturing Equipment

### Thank You!

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Visit my blog

www.hightechbizdev.com

for additional test resources.